TECHNICAL SPECIFICATIONS

Pulse Series

Power Ratings

Pulse 4x300	
Into 8 Ohms	170W
Into 4 Ohms	300W
Into 2 Ohms	330W
Pulse 2x650	
Into 8 Ohms	400W
Into 4 Ohms	650W
Into 2 Ohms	850W
Pulse 2x1100	
Into 8 Ohms	700W
Into 4 Ohms	1100W
Into 2 Ohms	1500W

Benefits of the Pulse Series

- **Very light weight**
- **Switched mode power supplies give solid performance at all power levels**
- **Microprocessor protection system**
- **Massive heatsinks for cooler operation and higher reliability**
- **Binding Post or Speakon output connector options**
- **Optional Remote control via C Audio CONNECT**
- **Internal crossover card options**

Cooler, Lighter, Stronger

The Pulse Series combines state-of-the-art switched mode power supplies to not only reduce amplifier weight by as much as 70% compared to conventional amps, but also to provide solid, consistent performance at all power levels.

Occupying just 2U of rack space, Pulse uses massive heatsinks and front-venting fans to keep the electronics really cool, plus a built-in microprocessor which continually monitors all the protection aspects of Pulse - these factors all dramatically enhance reliability.

Pulse amplifiers will perform for longer periods than conventional amplifiers at high output levels.

The combination of the switched mode PSU and a rugged steel chassis means inherent strength.

Technical Specifications

Power Ratings	**Pulse 4x300**	**Pulse 2x650**	**Pulse 2x1100**
Measured per channel, both channels driven at 1kHz to no more than 0.1% THD+N			
8 Ohms	170Wrms	400Wrms	700Wrms
4 Ohms	300Wrms	650Wrms	1100Wrms
2 Ohms	330Wrms*	850Wrms*	1500Wrms*
** Note: 2 Ohm spec is at 1% THD*			
Bridged Mono			
16 Ohms	400Wrms	800Wrms	1200Wrms
8 Ohms	600Wrms	1300Wrms	2200Wrms
4 Ohms	660Wrms*	1700Wrms*	3000Wrms*
** Note: 4 Ohm bridged spec is at 1% THD*			

Input Sensitivity	+1dBu for full output
Input Impedance	20kOhm
Distortion	<0.006% THD, 1kHz, 1dB below clip, 22kHz measurement bandwidth
Frequency Resp.	20Hz to 20kHz, +0/-0.2dB; <2Hz to >120kHz +0/-3dB
Controls	Power switch, bridge mode switching, indented level controls (these may be made tamper-proof)
Indicators	Mains present, Operate, Signal, Bridge, Clip, Overtemperature, Protect, Remote
Protection	Microprocessor supervised: overtemperature, DC on outputs, output stage overload, inrush current surge, mains fail and brownout.
Noise	<-100dB ref full output 20Hz - 20kHz measurement bandwidth
Slew Rate	>50 V/microsecond
Damping Factor	>200 ref 8 Ohm
Output Connectors	4x300 - Binding post or Speakon 2x650, 2x1100 - Binding post and Speakon
Power	115 or 230 volts AC nominal, internally selectable, 2000VA, all channels driven (4x300, 2x650); 3000VA (2x1100)
Dimensions - with rear rack ears	3.5" (89mm) x 18.2" (460mm) x 19" (483mm) depth 19.5", -21", 20" (494, 511, 530mm)
Weight	24lbs (11kg)

March 2000

Pulse P2X1100 circuit description

1. **switching power supply**
2. **power amplifiers**
3. **protection**
4. **frontpanel & flashing lights**
5. **PIC and system protection**

1. Switching Power Supply

Mains voltage is inserted via filtered IEC CN3. Earth is connected directly to chassis from the body of CN3. Live passes through fuse F2.
Live and Neutral pass though a further filter consisting of C2 (X2 rated), L1 - a common mode choke - and C15 & 14 (Y2 rated).
Live passes through the soft-start system, TH1, R14 and RLY1. R14 limits the initial current surge caused by the primary reservoir capacitors charging up. TH1 protects R14 if a fault causes excessive dissipation in R14. RLY1 shorts out TH1 and R14 when the PSU is running.

Live and Neutral then pass to bridge rectifier BR2 which, for the 230V setting full-wave rectifies mains, smoothing performed by reservoir capacitors C22,23,44,45,32,33. In the 115V setting, this power supply is configured as a voltage doubler. Thus, the High Tension (+HT) DC generated is approximately equal for 230V mains and 115V mains.

This will result in about 320Vdc between 'LIVE GND' and +HT. 'LIVE GND' is named as such because it is **not** isolated from mains but it is the reference point for the PSU. If you need to stick a scope probe around the primary side with the unit plugged in you must connect mains via an **Isolation Transformer**. Without this, at best you will only trip your RCD breaker, at worst you or your scope may not live to regret it. **Do not forget** that **320Vdc** is still pretty shocking whether it is isolated or not.

R36 and R37 ensure proper voltage sharing of the reservoir capacitors.

Power for the switching controller circuit is provided from two sources.
At start-up, the power comes from R93,113, ZD2, D22 and C75. C75 is charged up to about 47V through D22 from Zener regulator R93,113 and ZD2. The command to start the PSU comes from the PIC (+5V for off, 0V to switch on) via R33. The LED in OPT1 is turned on which turns the transistor on, shorting out pins 5&4. While the transformer windings are cooler than 120^0C the thermal cut-out (TX5-B) will be a short circuit. So R166 will be connected to the top of C75 and will form a Zener regulator with ZD9. The output of this zener regulator is buffered by TR49 which then powers the switching controller circuit.
C75 stores enough energy to run the controller for long enough until the second source of power is ready.
The second source of power comes from the transformer on pins 3 and 14. This secondary is voltage doubled by C82, D29,31 and C74 and produces about 48Vdc on VAUX. This is connected via D32 to the top of C75 so the controller circuit can continue running.
VAUX is used to directly power RLY1 to short TH1 and R14 out while the PSU is running.
The circuit comprising R165,R172,ZD10,R178,TR47 and R180 shut down the PSU when the voltage on C75 falls below about 32V. while the voltage on C75 is greater than 32V, TR47 is switched on and pulls pin10 of IC6 down to 0V which 'enables' IC6. When the voltage on C75 falls below 32V, TR47 switches off and pin10 of IC6 is pulled up to 20V through R180, 'disabling' IC6.
R92,8,85,C67,ZD3 and TR23 form a time delayed drive for RYL2. At start-up, RLY2 will be open and R127,145 will be in series with the primary of the transformer. These resistors limit the current surge caused by charging up the secondary reservoir capacitors C113,114,137,138. About 100ms after a successful start-up, TR23 will energise RLY2, shorting R127,145.

The switching controller circuit is based around IC6, and SG3525 PWM controller. Switching frequency is set by R175 and C199 to about 85kHz. R176 controls the 'dead time' period, setting it to between 500ns and 1μs. Outputs appear at pins11 and 14. These two outputs are complementary, that is when one is high (20V), the other is low (0V). Due to the dead time control, neither outputs are high at the same time but both are low for the 'dead time' period. These outputs are fed through R169,170 to high current buffers TR40,41 and TR42,43. The buffered outputs push-pull drive the primary of Pulse transformer TX4. R160 is a damping resistor used to minimise ringing caused by imperfections in TX4. The transformer has two secondaries, each driving one IGBT in anti-phase. The turns ratio is 1.5:1 (pri:sec) and due to the push-pull connection of the primary, the output of TX4 swings positive to about 15V to turn

the IGBT on, falls to 0V switching the IGBT off during dead time and falls to about -15V whilst the other IGBT is switched on.

IGBTs TR24,29 form a half bridge driver for TX5. D14,23 provide 'flyback' protection for TR24,29. These are not fitted as we are currently using IGBTs with integral 'flyback' diodes. Snubbers R84,C56,R117,C68 damp any ringing which may occur.
The drive for the transformer from the IGBTs is an 85kHz square wave almost hitting '+HT' at the top of it's travel and bottoming out slightly above 'LIVE GND'. This drive is connected to the primary of TX5 at pins 15&16. The other end of the primary at pins 1&2 connects to 'LIVE GND' through the closed RLY2 and C63,64,65.
C63,64,65 perform two important functions.

1. they prevent DC current flowing through TX5 thus preventing early saturation of the core.
2. they form a discontinuous resonant circuit with the leakage and stray inductance of the transformer. This means that the current will not be the same shape as the voltage. It is arranged that, for instance, positive current flow through TR24 will start from 0A, rise and fall in a half-sinusoidal fashion, reach 0A and stop before TR24 is switched off. This means that switching losses in the IGBTs are virtually eliminated because switching occurs whilst 0A of current is flowing.

There are two main secondaries.

1. Pins 10,11,4&5 are the low voltage centre tapped secondary winding. Output of this is full-wave rectified by D49,50,54,55 and smoothed by C126,C132. Further filtering is provided by L2,3 and C120,130 before passing to 15V regulator IC7 and -15V regulator IC8. The +15V and -15V outputs are 'decoupled' by C124,133 close to the regulators to ensure stability. C28 and C29 provide further 'decoupling' close to the option connectors CN11,12. D51 half-wave rectifies the secondary output. This is lightly smoothed by C117 and loaded by R219. This is passed via ZD15,R34,R35 and C25 to the PIC. While the PSU is running, this circuit will produce a digital 'high' at the PIC input. If the PSU stops for any reason, the small value of C117 means that the PIC will receive a digital 'low' well before any of the Power supplies have drooped significantly allowing the PIC time to prevent plops.
2. Pins … is the main Power centre tapped stacked secondary. This is full-wave rectified by C45,48,53,61,57,60,36,47 and smoothed by C113,137,138,114 to produce HT+, HT- and MT+, MT- so that MT+ is half HT+ and MT- is half HT-. R7,112 roughly equalise the discharge rate when the PSU is stopped.

2. Amplifier

Refer to channel 1

The amplifier consists of a 'Class A' driver and a 'Class AB' rail switched power output stage. The driver provides voltage gain only, the output stage provides current gain only.
Audio signal enters the amplifier through DC blocking capacitor C149, then low-pass filter R88 & C51 and onto the base of TR30. R261 provides a low source impedance in case the frontpanel board is disconnected. R89 provides a DC path to ground for the base current of TR30.
The output of the amplifier is fed-back through potential divider R104 and R102 to the base of TR31. C58 decouples the feedback signal at DC so that DC offsets generated by TR30,31 are not amplified at the output. D15,19 protect C58 in the event of a DC fault.
TR30 and TR31 form a Long Tailed Pair to amplify the difference between the input signal and the feedback signal. The gain of the LTP is reduced by R99 and R100 to help prevent oscillations and de-sensitise the performance of the input stage to parametric variations of the two transistors. A bias current of about 2.8mA for this LTP is provided through R98 from current source TR19, R57, D6,7 & R75. In the quiescent state half of this current is driven through each of TR30 and TR31. The collector current of TR30 and TR31 pass through ZD7 and ZD5 and are loaded through D27 and D26 by R137 and R146.
The outputs of TR30 and TR31 are taken from the anodes of D27 and D26 to the bases of another LTP - TR38 and TR37. C70 determines the frequency response to ensure stability. As before, R139 and R140 reduce the gain of this LTP and the bias current is set to about 8mA by R138. The collectors of TR37 and TR38 are loaded with a current mirror - TR20 & TR21 to maximise gain and provide a push-pull output.
Some of this output is fed-back to the base of TR31 through C63 and R103. This defines the open-loop frequency response independently of the output stage characteristics to ensure stability.
Finally, the Vbe multiplier - TR25, R82&83 - provides the output stage with two voltage signals which are identical except they are offset by a voltage varying between about 2.1V (heatsink hot) and 2.4V (heatsink cold). C53 ensures that the two offset signals are identical at AC.

The Current source consisting of TR19, R57, D6,7 and R75 determines the operating point of the whole class A driver. Therefore, one can mute the amplifier by switching this currrent source off.
The current source is switched off by TR18, R68 and C37. When TR18 is switched on, D6,7 are shorted out through R68 which mutes the current source. C37 is discharged in the process. When TR18 is switched off, C37 charges up through R75 until D6,7 are fully conducting which activates the current source.
TR18 is controlled by TR11, R56, R46, ZD1, R47 and R48.
If the PIC is absent or its +5V supply has failed the 'MUTE1' line will be in a high impedance state, i.e. nothing doing. The 4.7V reference supplied by R46 & ZD1 and emitter resistor R47 set the current through TR11 to about 200μA. This is enough to switch TR18 on and mute the amplifier. This is the default state.
When working, the PIC controls the state of the 'MUTE1' line. To mute the amplifier, the 'MUTE1' line is set to 0V. The current through TR11 is then set to about 4.2mA because R48 is now essentially in parallel with R47. This mutes the amplifier as before.
To activate the amplifier, the 'MUTE1' line is set to +5V. This, through R48, reverse biases the base-emitter junction of TR11. Thus TR11 is switched off as is TR18 so the amplifier becomes active.

Under normal conditions the signals at the bases of TR30 and TR31 will be the same. However, under fault conditions, such as a DC offset at the output, the base voltages will become offset also. For example, in the event of a large DC offset of +50V at the output, a positive DC voltage will appear at the feedback point and hence at the base of TR31. This DC voltage will make D65 conduct protecting C126, so the voltage at TR31 base should be 0.6 + 50V x R102/(R102+R104), about 4V. However, the important issue is that the voltage is **positive**. In the event the voltage is negative this indicates that the feedback divider is faulty. The voltage at TR31 base being positive whilst the base of TR30 is close to 0V will then reverse bias TR31 base-emitter, turning off the transistor. Therefore, no voltage should

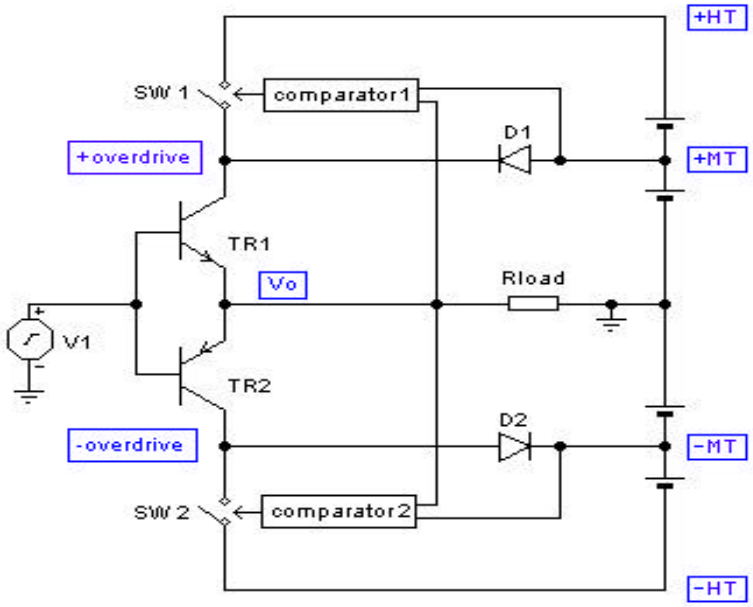
appear across R100 and R146 whilst double the normal voltage will appear across R99 and R137. Should this not be the case, it indicates a fault in the input stage itself.
The same process should now cause TR37 and TR20 &21 to be off and TR81 to be full on…

Class AB output stage

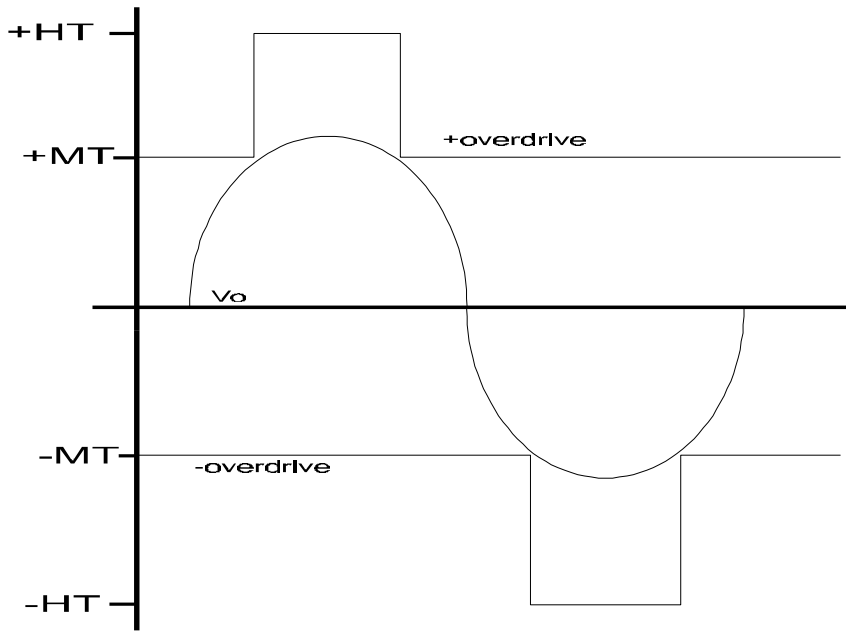
The input of the Output stage is loaded by C46. This defines the HF input impedance and thus averts very nasty oscillations that are caused by the variable, non-linear and sometimes negative raw input impedance. Resistors R60 and R182 ensure that output offsets are minimised when the amplifier is muted. D5 and D39 stop the Class A driver over-saturating TR12 and TR55. D11 and D40 prevent the output exceeding the power supply rails in the face of 'flyback' pulses from reactive loads.

The output stage consists of a symmetrical Siklai follower - TR12, TR13, R61, TR55, TR56, R181, R81, R80, C52, D13, D17 - generating the high current drive required for the parallel connected symmetrical follower output stage - TR26, TR14, TR34, TR46, R115, R94, R121, R124, TR72, TR59, TR88, TR79, R147, R141, R168, R159. V-I limiting is controlled by D8, D33, TR22, TR44, R96, R95, R116, R119, C60,R129, R149, R164, R163, C81, R64, C48, R128, C77, D10, D25, R212, R214, TR71, R217, R228, TR75.

The Pulse 2x1100 amplifier uses a rail switched (class G or commutated) output stage to increase efficiency. This works by effectively rolling two amplifiers into one, switching between them as required.



While Vo is between +MT and -MT, SW1 and SW2 are open and power is drawn from +MT and -MT through D1 and D2.
If Vo gets too close to +MT then comparator1 closes SW1. Power is now drawn directly from +HT and D1 is reverse-biased.
Similarly, if Vo gets too close to -MT then comparator2 closes SW2. Power is now drawn directly from -HT and D2 is reverse-biased.



1. Positive half-cycle

The output voltage is sensed at the top of current sharing resistor R124 to correct for errors caused by the varying voltage drop across current sharing resistors. This is divided down by R221 and R234 and enters pin6 of IC10-B which is used as a comparator. C123 compensates for time delay through the circuit. +MT is divided down by R229 and R230 and enters pin5 of IC10-B. R237 provides hysteresis around the comparator.
Whilst pin6 is lower than pin5, the output of the comparator is at +13.5V on pin7. This switches TR67 on with its collector current set by R216 to about 2.5mA.
When pin6 exceeds pin5, the output of the comparator goes to -13.5 on pin7. This switches TR67 off.

Rail switching is performed by FET1 and FET3 with commutation diode D52. FET1 and FET3 are connected in parallel except for the gates which have separate ‘gate stopper’ resistors R192, R195. A floating 10V supply for the drive circuit is provided by R199, ZD13 and C112. The drive circuit consists of push-pull buffer TR68,69, pull-up resistor R201 and C110.
When TR67 is on, 2.5mA flows through R201, dropping 12.75V. therefore, TR69 will be off and TR68 will be on, pulling FET1 and FET3 gates low which switches them off. Power for the amplifier thus flows from +MT through D52.
When TR67 is off, R201 pulls the bases of TR68,69 up, which pulls the gates of FET1 and FET3 up and switches them on. Power for the amplifier now flows from +HT through FET1 and FET3. C110 slows the rise and fall times of the +overdrive rail to about 1μs.

2. Negative half-cycle

The output voltage is sensed at the bottom of current sharing resistor R159 to correct for errors caused by the varying voltage drop across current sharing resistors. This is divided down by R207 and R248 and enters pin2 of IC10-A. C111 compensates for time delay through the circuit. -MT is divided down by R259 and R256 and enters pin3 of IC10-A. R246 provides hysteresis around the comparator.
Whilst pin2 is higher than pin3, the output of the comparator is at -13.5V on pin1. This switches TR74 on with its collector current set by R225 to about 2.5mA.
When pin2 exceeds pin3, the output of the comparator goes to +13.5 on pin1. This switches TR74 off.

Rail switching is performed by FET5 and FET6 with commutation diode D62. A 10V supply referenced to -HT for the drive circuit is provided by R239, ZD20 and C139.
The drive circuit consists of push-pull buffer TR81,82 pull-up resistor R251, C145 and current mirror TR80,D63,R258,R250.
When TR74 is on, the current mirror reflects 2.5mA through TR80 which pulls down on R251. Therefore, TR82 will be off and TR81 will be on, pulling FET5 and FET6 gates low which switches them off. Power for the amplifier thus flows from -MT through D62.
When TR74 is off, the current mirror reflects this by turning TR80 of. R201 pulls the bases of TR81,82 up, which pulls the gates of FET1 and FET3 up and switches them on. Power for the amplifier now flows from -HT through FET5 and FET6. C145 slows the rise and fall times of the -overdrive rail to about 1μs.

3. Protection

Output stage

Output stage protection is accomplished by a three-slope V-I limiting circuit which has limiting characteristics chosen to emulate the Safe operating area of the output stage transistors at their maximum operating temperature.
As the output stage is symmetrical, the positive half only will be described.
The V-I limiting works by controlling TR22: when the base-emitter voltage of TR22 exceeds about 0.65V then TR2 turns on and steals current, via D8, from the input of the output stage and thereby limiting the output. So, V-I limiting is controlled by controlling the base-emitter voltage of TR22.
Each output device has its own current sharing resistor - R115 R94, R121, R124 - the voltage across which is proportional to the current flowing in the output device. These voltages are sampled and summed by R96, R95, R116 and R119. C60 improves stability when V-I limiting is activated.
Thus the amplifier is protected for short circuits because the base-emitter voltage of TR22 reaches 0.65 if the output current is large and the output voltage is less than about 1Vpk
For output voltages exceeding about 1Vpk, D10 conducts connecting R212, R214 & TR71 to sense the output voltage. In this case, as output voltage increases, the base-emitter voltage of TR22 reduces, thus the current limit is increased as the output voltage increases, defining the 2^{nd} slope of the limiting characteristic.
The third slope is controlled by TR71, R214 and the rail switching comparator. If the +overdrive rail is low, then TR71 is switched on and shorts R214, leaving R212 to define the 2^{nd} slope. When the +overdrive is high, TR71 is switched off and the 3^{rd} slope is defined by R214 in series with R212.
C48 and R64 desensitise the current allowing brief peaks of output current which exceed the normal current limited amount to allow proper operation into reactive loads (ie loudspeakers).

Excessive continuous power demand

Continuous maximum sine-wave operation of both channels into the minimum rated load resistor is beyond the capabilities of this product and is treated as a fault condition.
Refer to channel1
Amplifier output current is measured by R159, 124, 183, 191, 177, 179 and IC5-A.
Output current causes a voltage drop across current sharing resistors R124 and R159. If the voltage across both resistors is measured, positive output current will cause the voltage to increase and negative output current will also cause the voltage to increase. This is sensed and attenuated by differential amplifier R183, 191, 177, 179 and IC5-A.
The output at pin1 of IC5-A is the sum of: 1. full-wave rectified replica of the output current; 2. An error signal caused by incomplete common-mode rejection. The error signal is merely attenuated output voltage.
As the desired signal, output current, has been full wave rectified and the undesired signal, output voltage, has not, the undesired signal can be removed without corrupting the desired signal by passing it through an integrator. The raw output current signals from each channel are summed, averaged and inverted by R174, 52, 53, C43 and IC4-A (sheet 4) so that the output at pin1 of IC4-A is a negative DC voltage proportional to the total average output current.
This voltage is compared with a threshold, set by R50 and R51 to about
-2.7V, at IC4-B. R55 provides hysyteresis. If it is higher than the threshold, pin7 will swing to -13.5V. If it is lower than the threshold then pin7 will swing to +13.5V.
IC4-B pin7 drives transistors TR66, 64, 65 and 63. The collectors of these transistors connect to the collectors of TR67, 86, 74& 62. When pin7 swings to +13.5V, TR66, 64, 65& 63 are switched on, the current flow set to 2.5mA by R198 and R197. This forces rail switching off.
IC4-B pin7 is connected to the PIC pin22 through R49.

Bridge imbalance protection.

During normal operation, the bridged output is fully differential mode with little or no common-mode signal component. Activation of the output stage current limiters erratically upsets this state, producing a large common-mode error - imbalance - which can destroy the output stages.
The bridge imbalance detection is performed by R10,12,13, TR3 and R11.
In two channel mode, the 'BRIDGE 1+2' line is pulled up to about +13V. this switches TR3 on through R11. The collector of TR3 is connected to pin 23 of IC1 (PIC). The input of the PIC is internally protected by diodes against inputs above +5V and below 0V. so, in two channel mode, pin23 of IC1 receives no signal.
In bridge mode, the 'BRIDGE 1+2' line is held at 0V which switches TR3 off. Now pin 23 of IC1 can receive a signal. R10, 12 sum the output of each channel, the result appearing across R13 which sets the sensitivity. If the bridge is balanced, the voltage across R13 will be zero. If the bridge is unbalanced then there will be voltage across R13 which is also connected to pin23 of IC1.
When an imbalance is detected the PIC immediately mutes both channels for 4 seconds. Then the channels are re-activated.

DC Protection

Each channels output is connected through R16,R15 to R21 and C16. C16 ensures that only DC is detected.
For no DC fault, R32 pulls pin9 of IC1 towards +5V.
For a positive DC faults, D4 becomes forward biased and turns TR8 on, pulling pin9 of IC1 (PIC) towards 0V.
For a negative DC fault, D3 becomes forward biased which switches TR10 and TR9 on, pulling pin9 of IC1 (PIC) towards 0V.
In the event of a DC fault, the PIC switches the PSU off, waits and then tries again.
C30,31,35,36 prevent the full-wave recification of PSU noise causing false alarms.

4. Frontpanel and small signal circuits

Refer to channel 1

Audio signal enters the amplifier on CN1, CN5, CN8 or CN10 in balanced form, positive phase - 'hot' - on pin 2 of CN8 and negative phase - 'cold' - on pin 3. The signals on each leg will always be out of phase but will not necessarily equal in amplitude. This signal passes through RF1 and RF2 which shunt RF rubbish to chassis. R1 and R4 prevent thumps due to connection / re-connection. TX1 is an optional audio coupling transformer which is normally not fitted and bypassed by LK2 and LK3. The signal then passes through dc blocking capacitors C3 and C9, through links fitted in the option connectors CN11 and CN12 and on to the frontpanel board via pins 1&2 of CN17.

The balanced signal is converted to single-ended by IC1-A (pins1,2,3) and R1,2,3,4,52,59 which form a standard differential amplifier. C25 and C26 shunt HF energy to ground.
The signal exits pin1 of IC1-A and is routed to two places, one being the signal led circuit (described later) the other being the level control P1, R5 and analogue switch IC2-A. P1 is a standard linear 10k pot rather than a log taper pot. The level control is given an 'audio' taper (a compromise between log taper and linear taper) by R5 so that the level is attenuated by 10dB at the centre position (rather than 6dB for linear or 20dB for log). The analogue switch is normally closed (pin1 of IC2 low - 0V) allowing operation of the level control. In remote controlled operation (with the remote option installed) the level control is disabled by pulling pin1 of IC2 high (+15V) thus opening the switch.

Up to this point channel1 and channel2 have identical function. What happens next is determined by the bridge switch (rear panel).

1. bridge mode off

the 'bridge1+2' signal line will be held high by R49 and LD9. Although LD9 will not be illuminated, enough current flows to pull pins 8 & 9 of IC2 high. This opens the switches IC2-C (pins 10 &11) and IC2-D (pins 6 & 7).
Channel 1 signal enters pin 5 of IC1 which is configured to have a gain of +14.5dB by R17, R15 and continues through R7 to pin13 of CN1.
Channel 2 signal enters pin 5 of IC3 which is configured to have a gain of +14.5dB by R30, R16 and continues through R14 to pin15 of CN1.

2. bridge mode on

the 'bridge1+2' signal line will be held low by the rear panel bridge switch. LD9 will be illuminated and pins 8 & 9 of IC2 will be pulled low (0V). This closes the switches IC2-C (pins 10 &11) and IC2-D (pins 6 & 7).
Channel 1 signal enters pin 5 of IC1 which is configured as a to have a gain of +14.5dB by R17, R15 and continues through R7 to pin13 of CN1.
Closure of switch IC2-C connects this signal to pin6 of IC3 through R29 which, in conjunction with R30, configures IC3-B to be a unity gain inverter (R16 does not affect the signal gain). Thus, the channel1 signal is inverted and passed to channel 2 through R14 to pin15 of CN1.
Channel 2 signal is shorted to ground through switch IC2-D.

Signal LED

The signal is coupled from pin1 if IC1 through C10 and across R35 to IC8 pin3.
Initial conditions: C15 has 0V across it and LD1 is off. Pins 1,2 and 3 of IC8 are at 0V.
A signal appears at pin3 of IC8. It is moving from 0V in a positive direction. Due to the large open-loop gain of IC8, pin1 will move in a positive direction at a much greater rate. This will forward bias the diode in D1 (which connects pin1 to the top of C15) and charge up C15.
When enough volts have accumulated on C15, LD1 will conduct, its current limited by R34 and R33. R34 and R33 also form a potential divider applying negative feedback to pin2 thus setting the sensitivity of the circuit.

The signal at pin3 of IC7 now moves in a negative direction. Therefore pin1 will move negative at a much greater rate and the diode in D1 (which connects pin1 to the top of C15) becomes reverse biased. The other diode in D1 (connecting pin1 to pin2) now conducts preventing saturation of the op-amp. LD1 will continue to glow by discharging C15 until the voltage on C15 falls below that required to turn LD1 on.

Clip LED

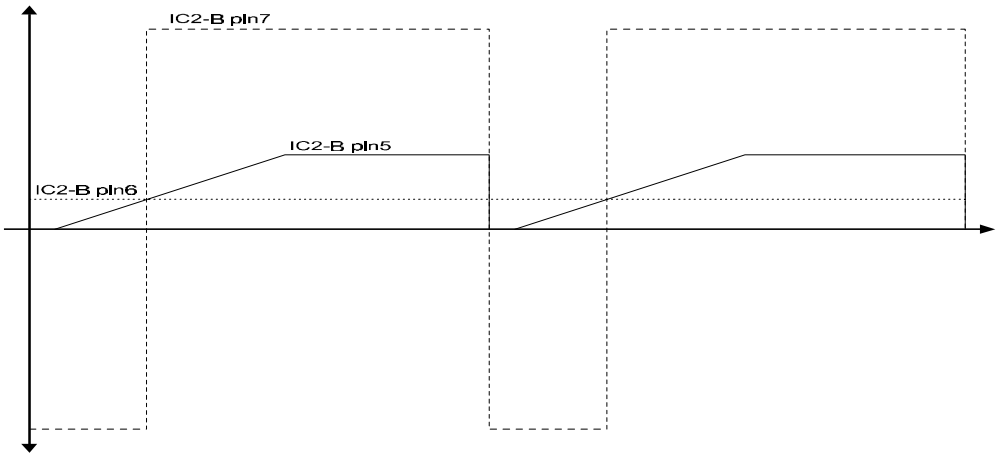
The clip detector circuit is on the main board consisting of IC5-B, R87,148,101,153,158 & R173 and C89&93. These are connected to form a differential amplifier which samples the voltage between the base of TR30 and the base of TR31. This voltage is the difference between the input and the divided down output of the amplifier. When the amplifier clips, there is a large difference between the input and the divided down output which is amplified by the differential amplifier. This passes from pin1, through R173 to pin 23 of CN17 and onto the frontpanel board. Here it is full-wave rectified by D5 and D6, smoothed by C17 and the resultant voltage illuminates LD5 through R45.

5. System management

Power for the management system is provided by a conventional transformer-rectifier-capacitor-regulator supply.
TX3 receives mains through F1 and is not affected by the main chassis fuse (F2). The secondary passes through fuse F3 to bridge rectifier BR1. The rectified AC is then smoothed by C11 producing about $25V_{dc}$ for $230V_{ac}$ mains or $12.5V_{dc}$ for $115V_{ac}$ mains.
The regulator circuit used is similar to the internal workings of an LM317. TR1 and TR2 form a darlington pass transistor. R9 provides bias current for D1, a TL431. D1 combines a voltage reference of 2.5V and an amplifier in one package. C6 prevents oscillations. R5 and R6 set the output voltage to 5V - 2.5V x (1+R5/R6).

The brain behind the operations is IC1, a MICROCHIP PIC16C57 microprocessor. This is **not** a re-programmable part. The clock is set to 3.58MHz by XT1, C19, C17 and pins27, 28 of IC1.

Each of the heatsinks has an LM35DZ, IC11 and IC12, attached close to the front of the unit. The voltage at pin2 of each of these gives a measurement of the temperature - 10mV per ^{0}C starting at 0V for 0^{0}C. Continuing with channel1, the temperature signal is filtered by R263 and C26 and enters pin3 of IC2-A. this is configured to give a gain of x10.2 giving 102mV per ^{0}C. The output at pin1 of IC2-A is coupled through R42 to pin24 of CN11. It is also coupled through potential divider R38, R39 to pin 6 of IC2-B at which point the signal is 34mV per ^{0}C. IC2-B (pins 5, 6, 7), R45, C34, R27 and IC1 pins 6, 7 comprise an analogue to digital converter. At the start of conversion, pin6 of IC1 is set to 0V for 1ms and discharges C34 through R27. Pin 6 of IC1 is then set to high impedance mode. At this point, pin7 of IC2-B is at -13.5V because pin5 is at a lower voltage than pin6. Now, the voltage on C34 ramps at about 600mV/ms because it is being charged by R45. The ramp stops at about 5.5V, limited by the protection diode on pin6 of IC1. The voltage on C34 is connected to pin5 of IC2-B so that when the ramp voltage exceeds the temperature voltage on pin6, pin7 changes to +13.5V. pin7 is connected to pin7 of IC1 through R31. In this way, the IC1 has a measure of time between the start of conversion and when pin7 (IC1) receives a logic 'high' which is proportional to the voltage at pin6 of IC2-B. After 18.32ms the conversion cycle starts again.



The heatsink temperature measurements are used to control the fan speed and to mute overheating channels.
Take, for instance, channel 1. If the heatsink temperature exceeds 90^{0}C then channel 1 is muted. Channel 1 will be re-activated when the heatsink temperature falls below 75^{0}C.
The two fans are connected in parallel, the negative wires connected to -15V, the positive wires connected through R17 to R18 and the collector of TR6. If the heatsink temperature is less than 55^{0}C then pin17 of IC1 (PIC) is set to +5V. This turns TR5 on which in turn switches TR6 off leaving the fans powered through R18. If the heatsink exceeds 55^{0}C then pin17 of IC1 is set to 0V, switching TR5 off and therefore TR6 on so that TR6 shorts R18 out. The fans are returned to slow speed when the heatsink temperature falls below 50^{0}C. TR4 and TR7 are used to completely switch the fans off when a brown-out condition is detected.

DRAWING NUMBER ISSUE

S-C300AS-05

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Tel 01707 660667
Fax 01707 660755

TITLE:
PULSE 4x300 AMPLIFIER
SHEET 1

FILENAME: S-C300AS-05.SCH

DRAWN: BPV

DATE: 12-01-99

CHECKED:

MATERIAL:

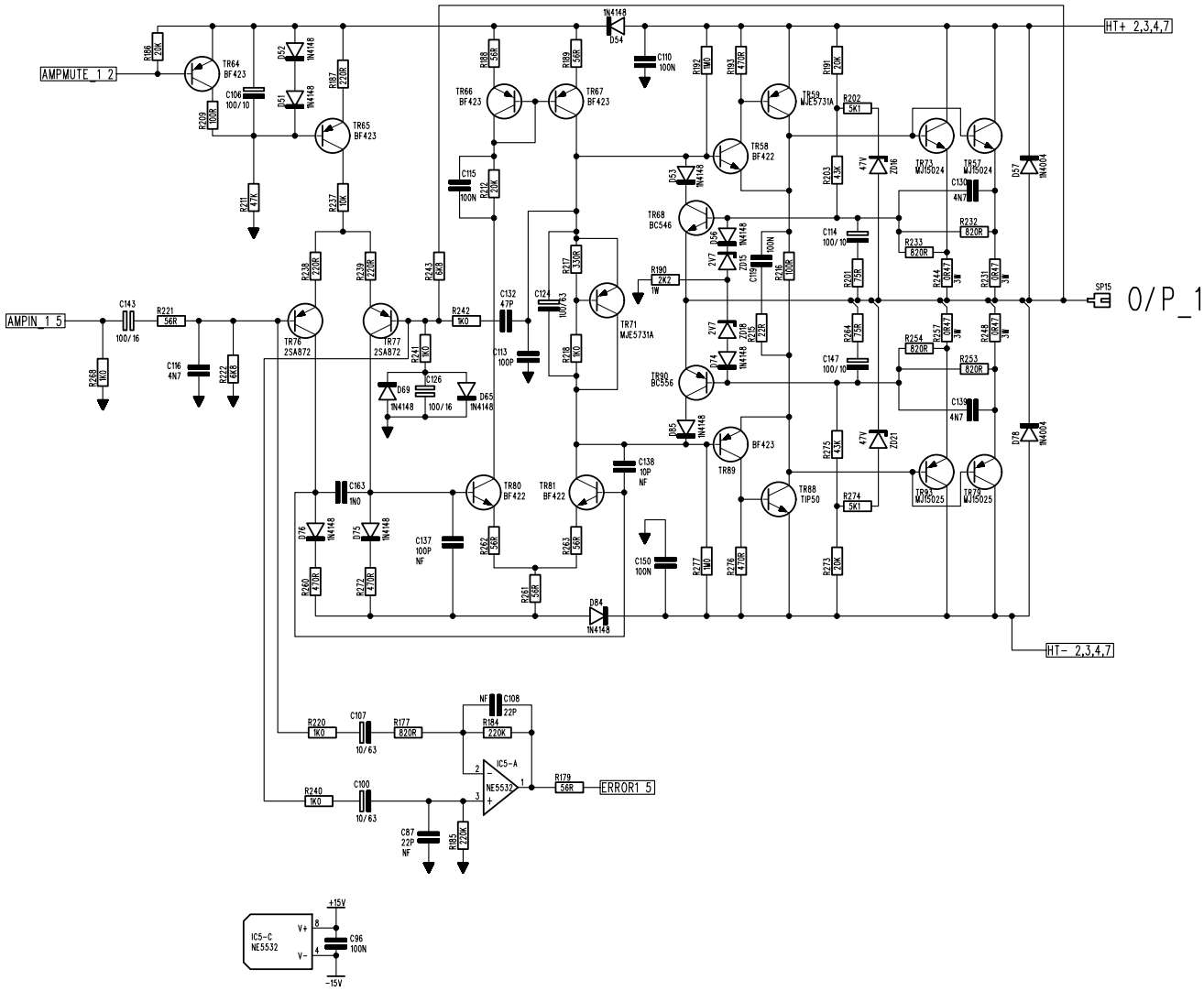
FINISH:

ISSUE COMMENTS:

1. PRODUCTION RELEASE 12-08-98
2. ECN0128 12-01-99
3. ECN0150 19-04-99
4. TX7 CIRCUIT SYMBOL UPDATED

4a. ECN0190 12-07-99
4B. ECN0251 15/11/99
4c. ECN0624 03/12/99
4D. ECN0275 11/01/00
5. ECN0333 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C300AS-05

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TITLE:
PULSE 4x300 AMPLIFIER
SHEET 2

FILENAME: S-C300AS-05.SCH

DRAWN: BPV

DATE: 12-01-99

CHECKED:

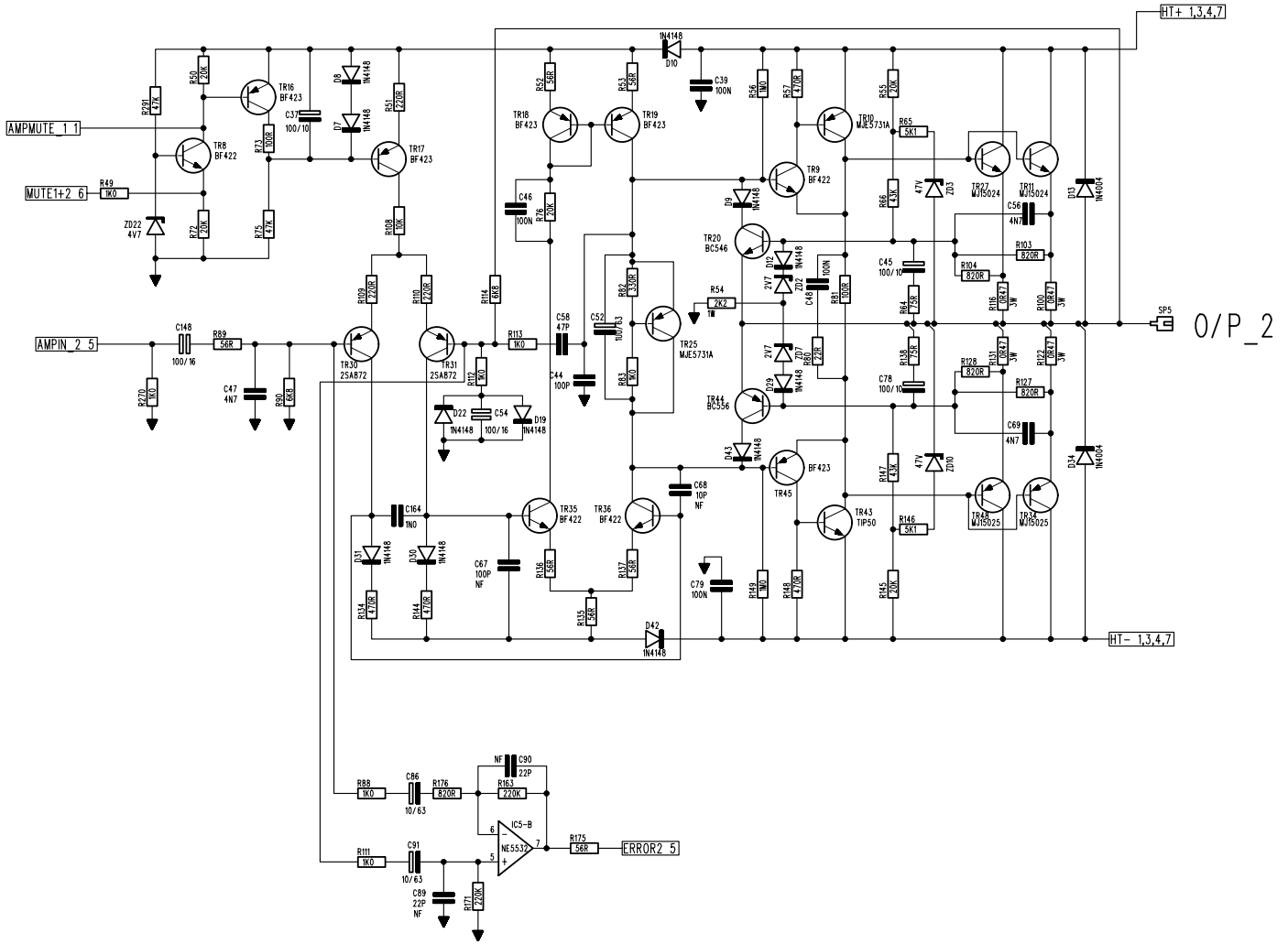
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRODUCTION RELEASE 12-08-98
2. ECN0128 12-01-99
3. ECN0150 19-04-99
4. TX7 CIRCUIT SYMBOL UPDATED
4a. ECN0190 12-07-99
4B. ECN0251 15/11/99
4c. ECN0624 03/12/99
4D. ECN0275 11/01/00
5. ECN0333 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C300AS-05

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TITLE:
PULSE 4x300 AMPLIFIER
SHEET 3

FILENAME: S-C300AS-05.SCH

DRAWN: BPV

DATE: 12-01-99

CHECKED:

MATERIAL:

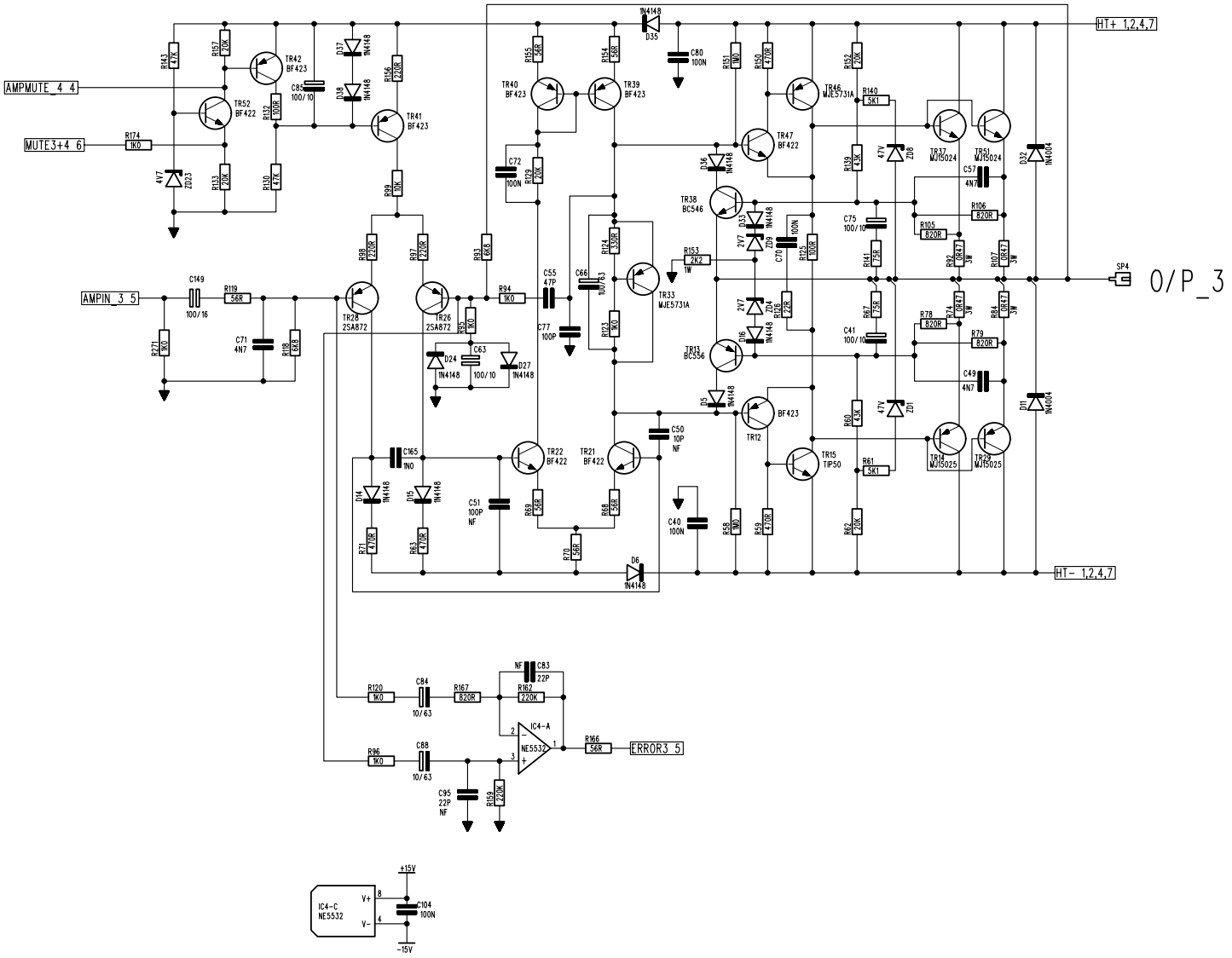
FINISH:

ISSUE COMMENTS:

1. PRODUCTION RELEASE 12-08-98
2. ECN0128 12-01-99
3. ECN0150 19-04-99
4. TX7 CIRCUIT SYMBOL UPDATED

4a. ECN0190 12-07-99
4B. ECN0251 15/11/99
4c. ECN0624 03/12/99
4D. ECN0275 11/01/00
5. ECN0333 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C300AS-05

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TITLE:
PULSE 4x300 AMPLIFIER
SHEET 4

FILENAME: S-C300AS-05.SCH

DRAWN: BPV

DATE: 12-01-99

CHECKED:

MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRODUCTION RELEASE 12-08-98
2. ECN0128 12-01-99
3. ECN0150 19-04-99
4. TX7 CIRCUIT SYMBOL UPDATED
4a. ECN0190 12-07-99
4B. ECN0251 15/11/99
4c. ECN0624 03/12/99
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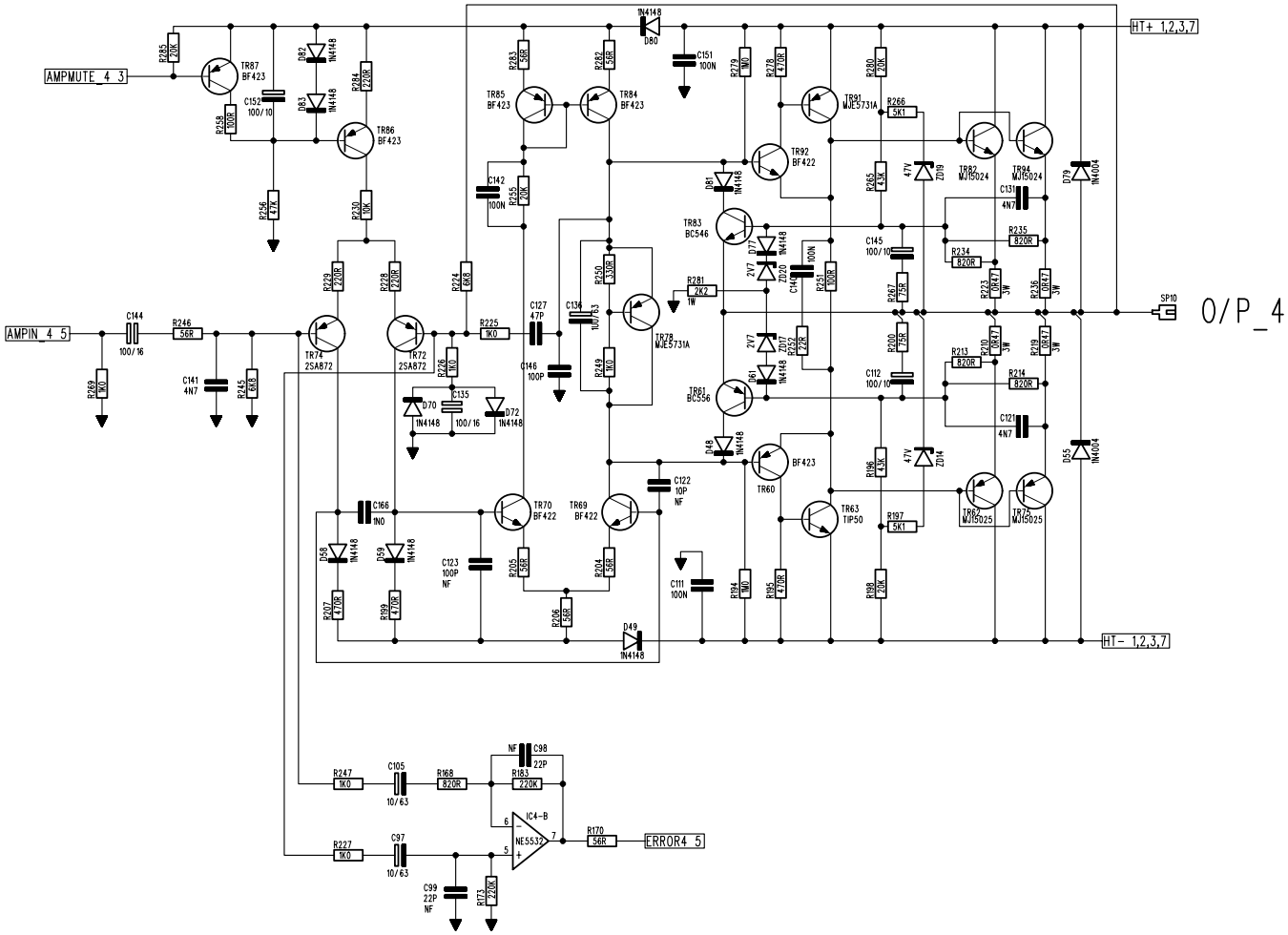
PART NUMBER:



DRAWING NUMBER ISSUE

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TITLE:
PULSE 4x300 AMPLIFIER
SHEET 5

FILENAME: S-C300AS-05.SCH

DRAWN: BPV

DATE: 12-01-99

CHECKED:

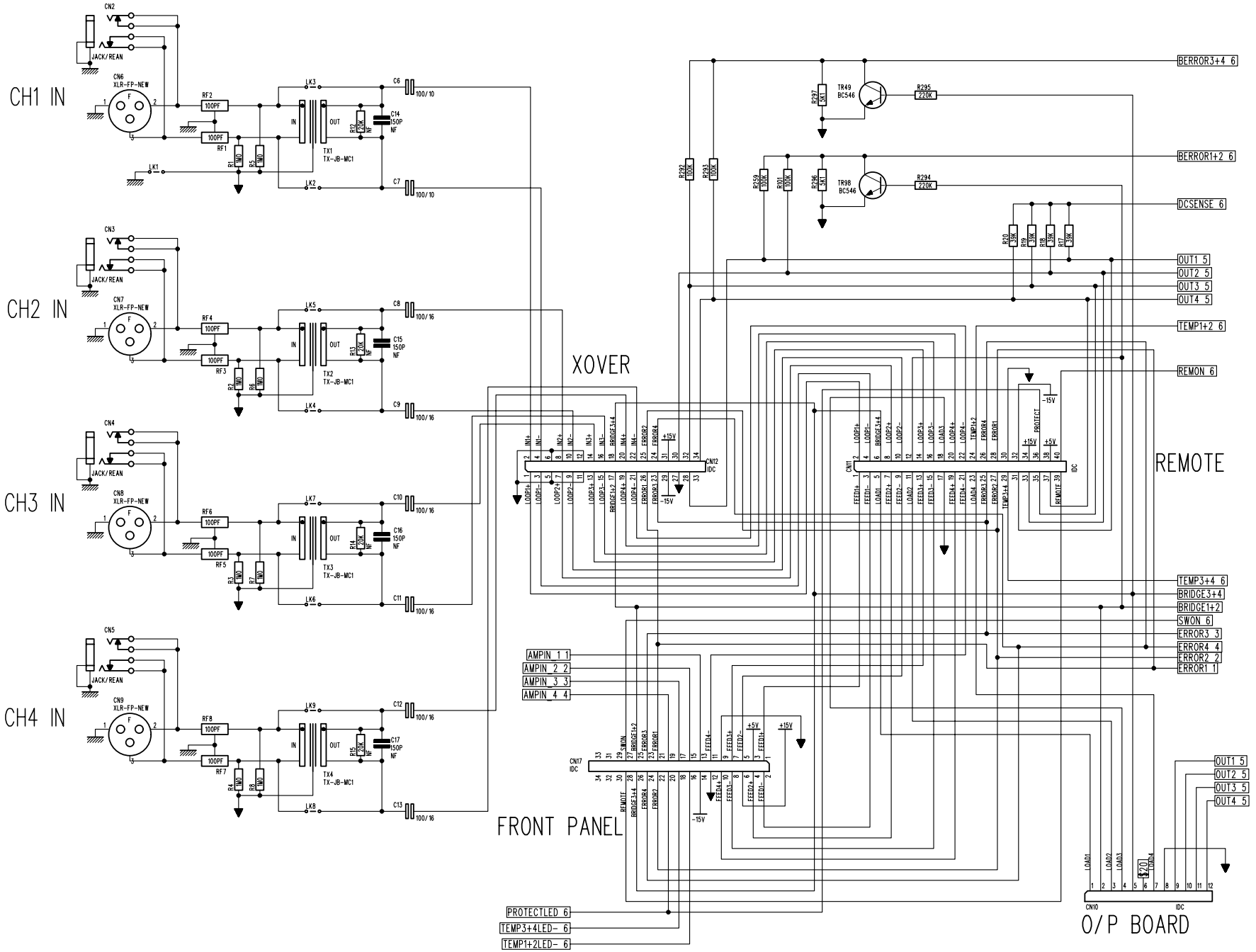
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRODUCTION RELEASE 12-08-98
2. ECN0128 12-01-99
3. ECN0150 19-04-99
4. TX7 CIRCUIT SYMBOL UPDATED
4a. ECN0190 12-07-99
4B. ECN0251 15/11/99
4c. ECN0624 03/12/99
4D. ECN0275 11/01/00
5. ECN0333 05/05/00

PART NUMBER:



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TITLE:
PULSE 4x300 AMPLIFIER
SHEET 6

FILENAME: S-C300AS-05.SCH

DRAWN: BPV

DATE: 12-01-99

CHECKED:

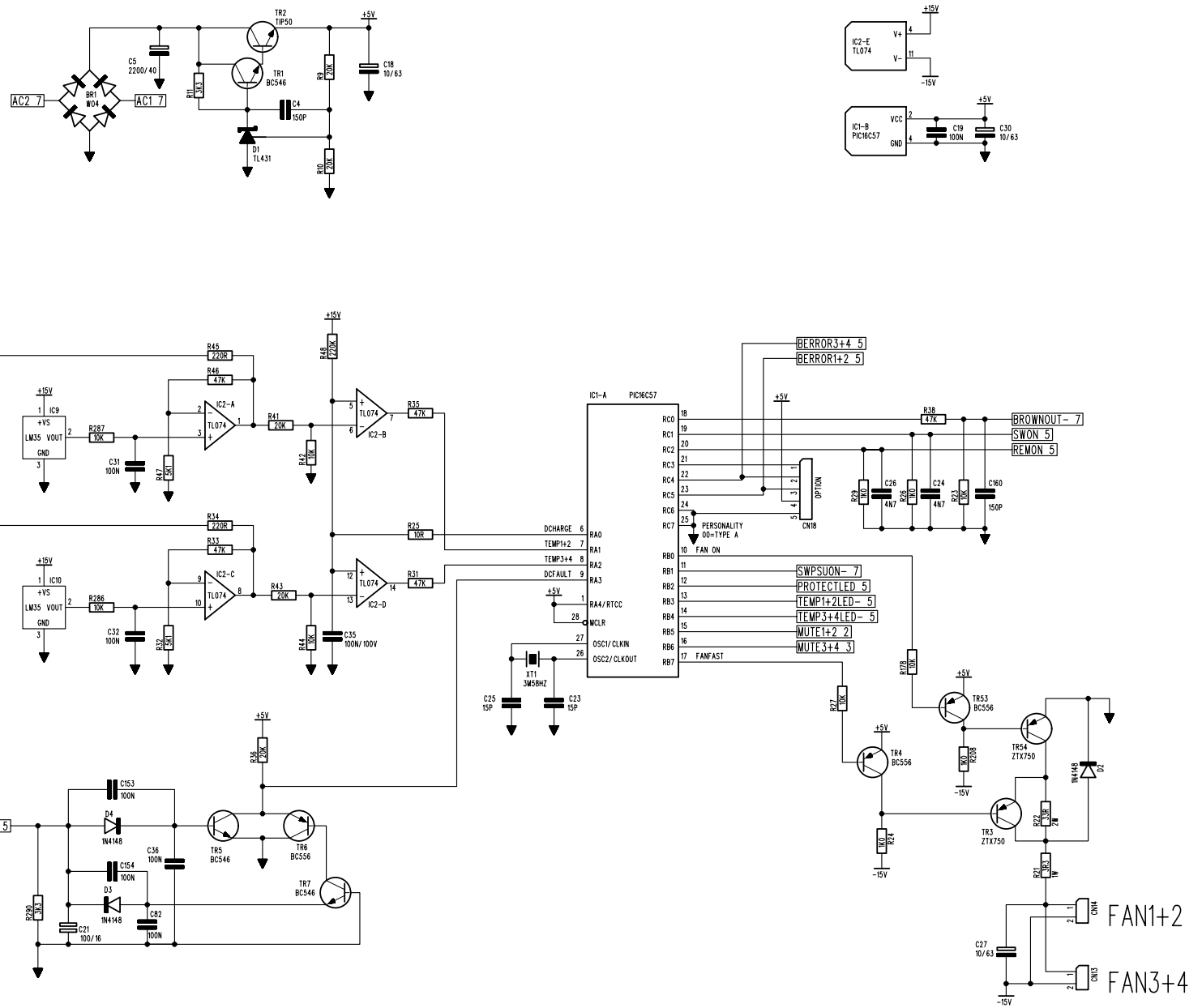
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRODUCTION RELEASE 12-08-98
2. ECN0128 12-01-99
3. ECN0150 19-04-99
4. TX7 CIRCUIT SYMBOL UPDATED
4a. ECN0190 12-07-99
4B. ECN0251 15/11/99
4c. ECN0624 03/12/99
4D. ECN0275 11/01/00
5. ECN0333 05/05/00

PART NUMBER:



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TITLE:
PULSE 4x300 AMPLIFIER

SHEET 7

FILENAME: S-C300AS-05.SCH

DRAWN: BPV

DATE: 12-01-99

CHECKED:

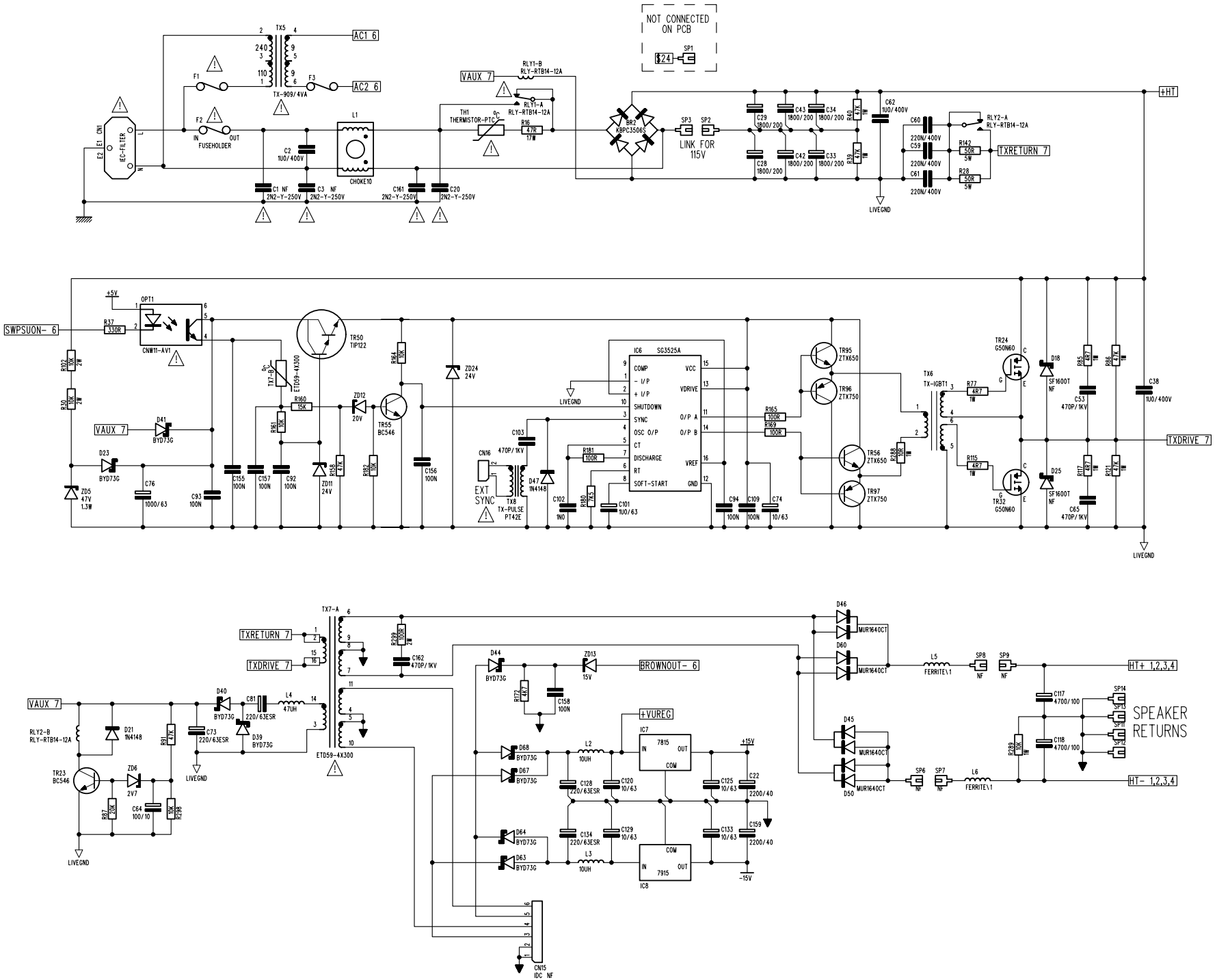
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRODUCTION RELEASE 12-08-98
2. ECN0128 12-01-99
3. ECN0150 19-04-99
4. TX7 CIRCUIT SYMBOL UPDATED
4a. ECN0190 12-07-99
4B. ECN0251 15/11/99
4c. ECN0624 03/12/99
4D. ECN0275 11/01/00
5. ECN0333 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C300BS-03

HARMAN INTERNATIONAL
INDUSTRIES LIMITED
CRANBORNE HOUSE
CRANBORNE ROAD
POTTERS BAR
HERTS
EN6 3JN
Tel 01707 660667
Fax 01707 660755

TITLE: PULSE 4 x 300
FRONT PANEL

SHEET 1 of 1

FILENAME:

DRAWN: BPV

DATE: 12-04-99

CHECKED:

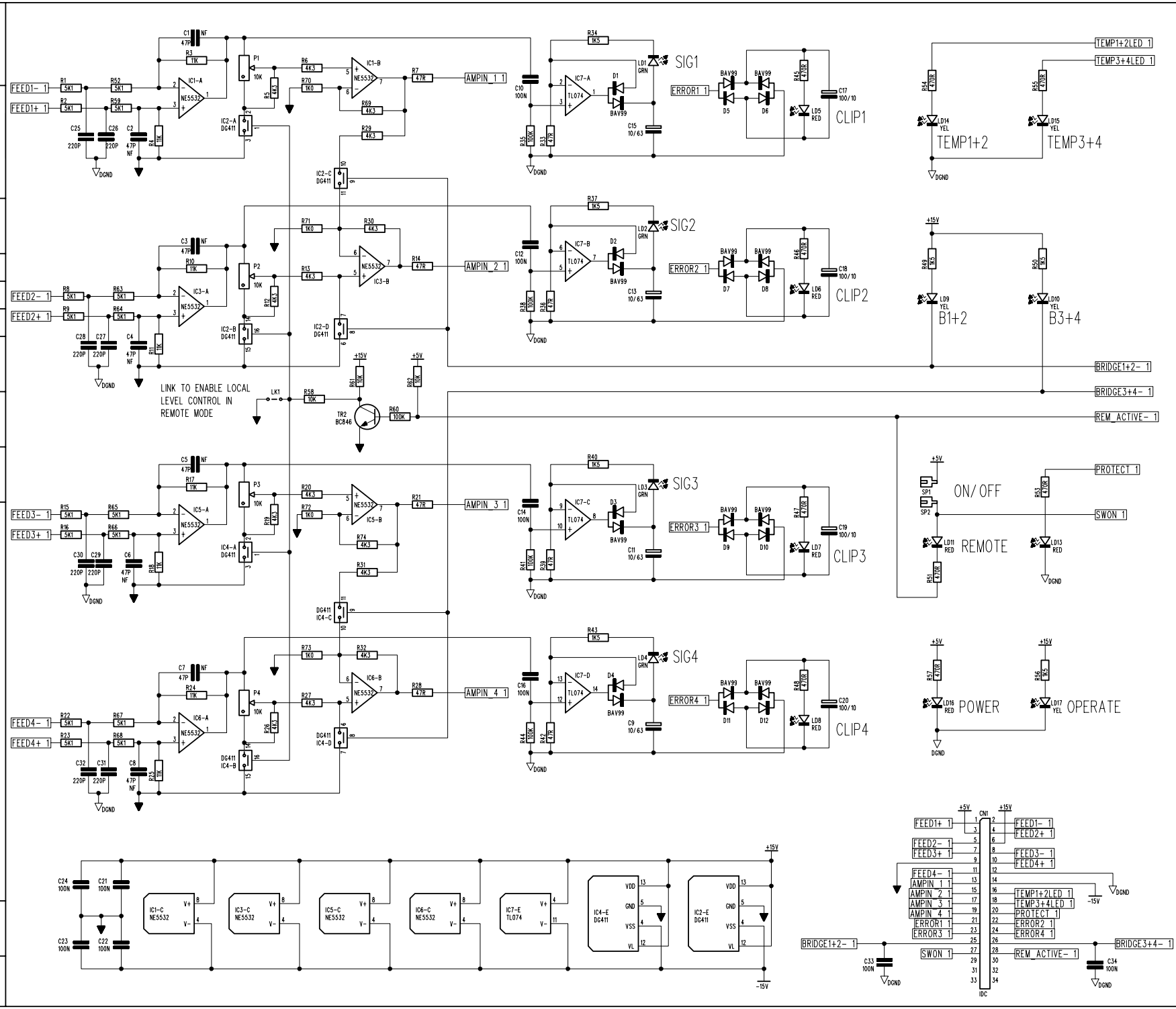
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRODUCTION RELEASE 12-08-98
2. ECN0128 12-01-99
2a. ECN0186 12-07-99
3. ECN0331 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C650AS-03

HARMAN INTERNATIONAL
INDUSTRIES LIMITED
CRANBORNE HOUSE
CRANBORNE ROAD
POTTERS BAR
HERTS
EN6 3JN
Tel 01707 660667
Fax 01707 660755

TITLE:

PULSE 2x650 AMPLIFIER

SHEET 1

FILENAME:

DRAWN: BPV

DATE: 04/01/00

CHECKED:

MATERIAL:

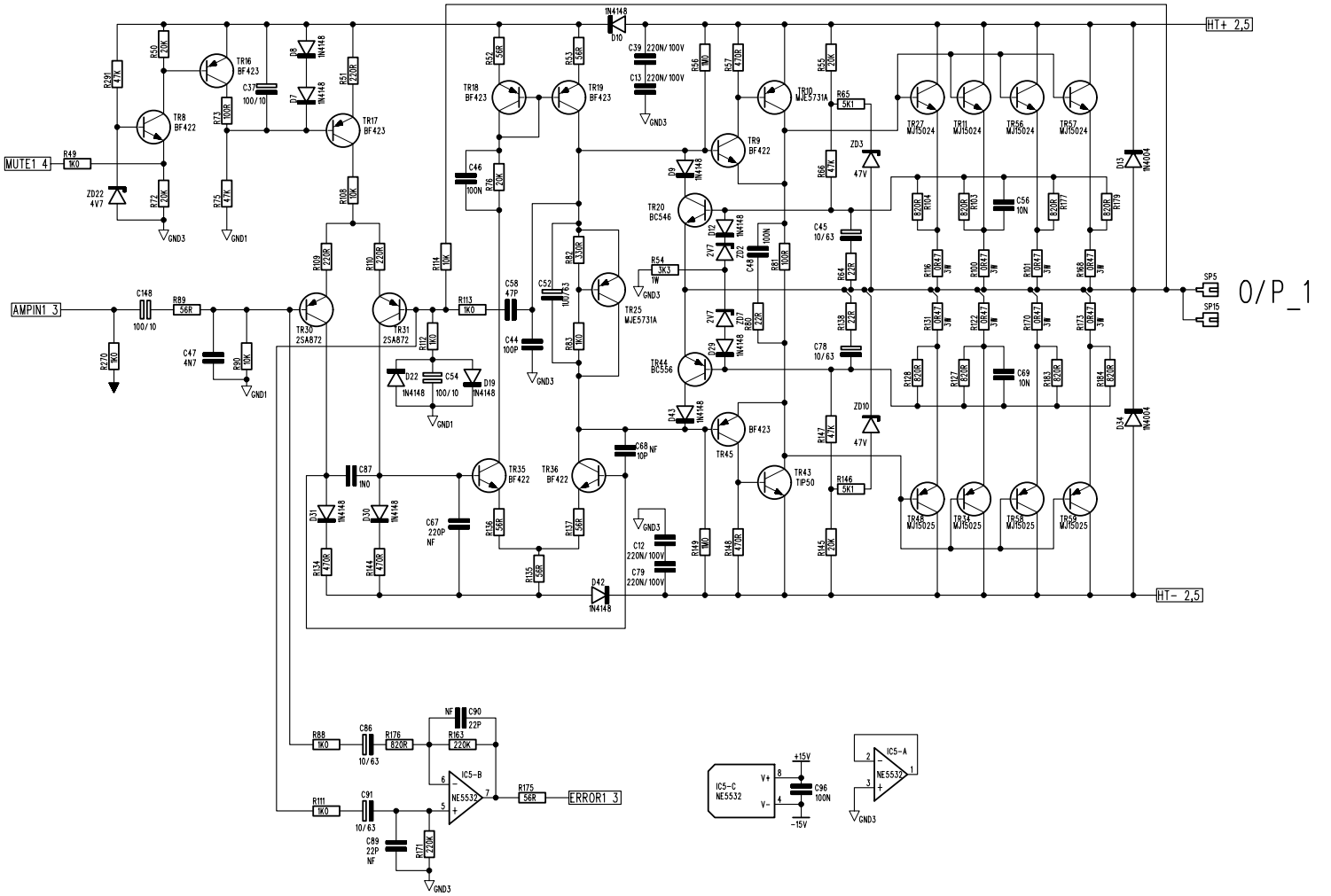
FINISH:

ISSUE COMMENTS:

1. PRE-PRODUCTION RELEASE 10-05-99
2. PRODUCTION RELEASE 22-06-99

2A. ECN203 02/09/99
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
3. ECN0334 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C650AS-03

HARMAN INTERNATIONAL
INDUSTRIES LIMITED
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CRANBORNE ROAD
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TITLE: PULSE 2x650 AMPLIFIER

SHEET 2

FILENAME:

DRAWN: BPV

DATE: 04/01/00

CHECKED:

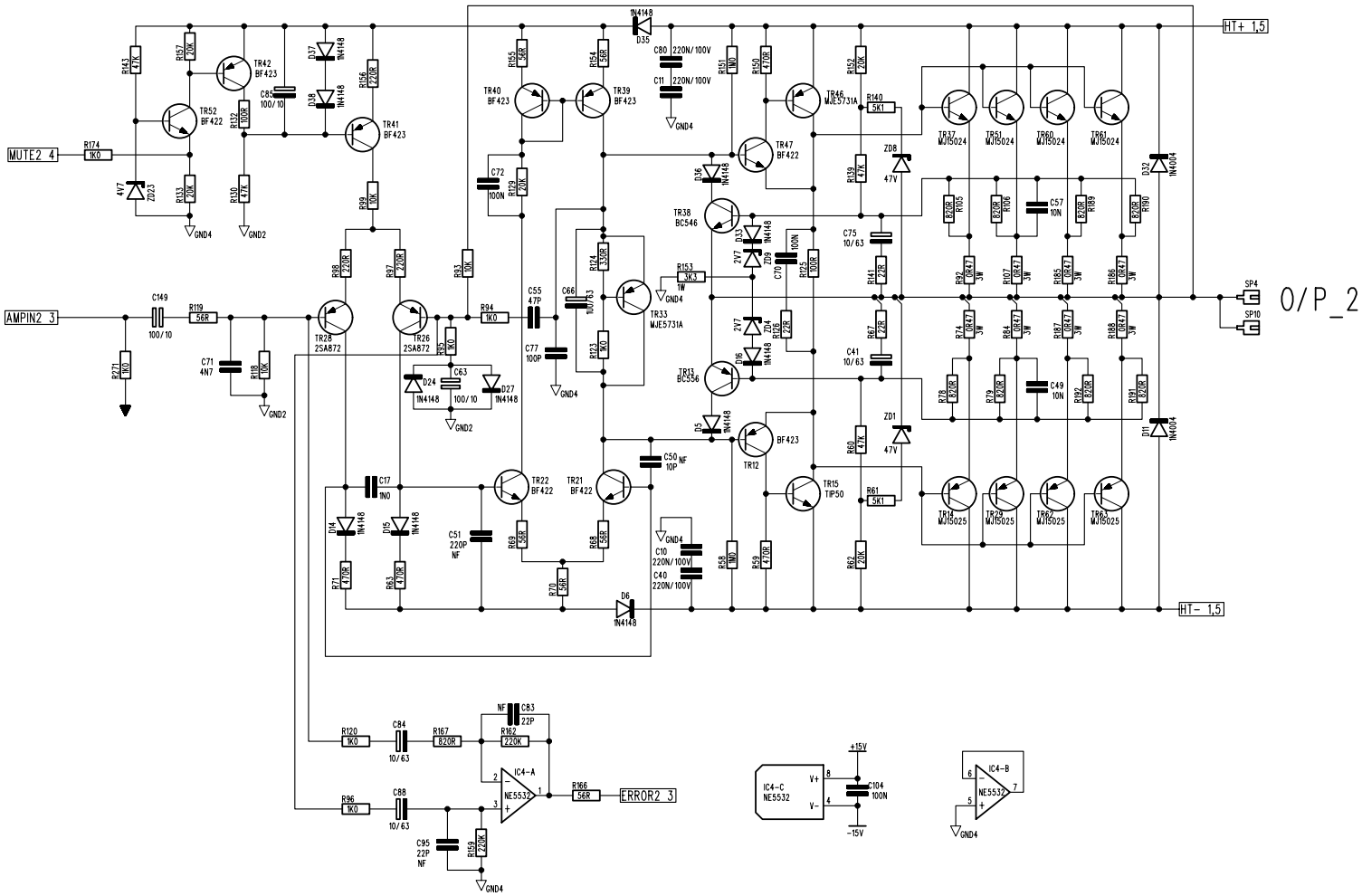
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRE-PRODUCTION RELEASE 10-05-99
2. PRODUCTION RELEASE 22-06-99
2A. ECN203 02/09/99
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
3. ECN0334 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C650AS-03

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TITLE: PULSE 2x650 AMPLIFIER

SHEET 3

FILENAME:

DRAWN: BPV

DATE: 04/01/00

CHECKED:

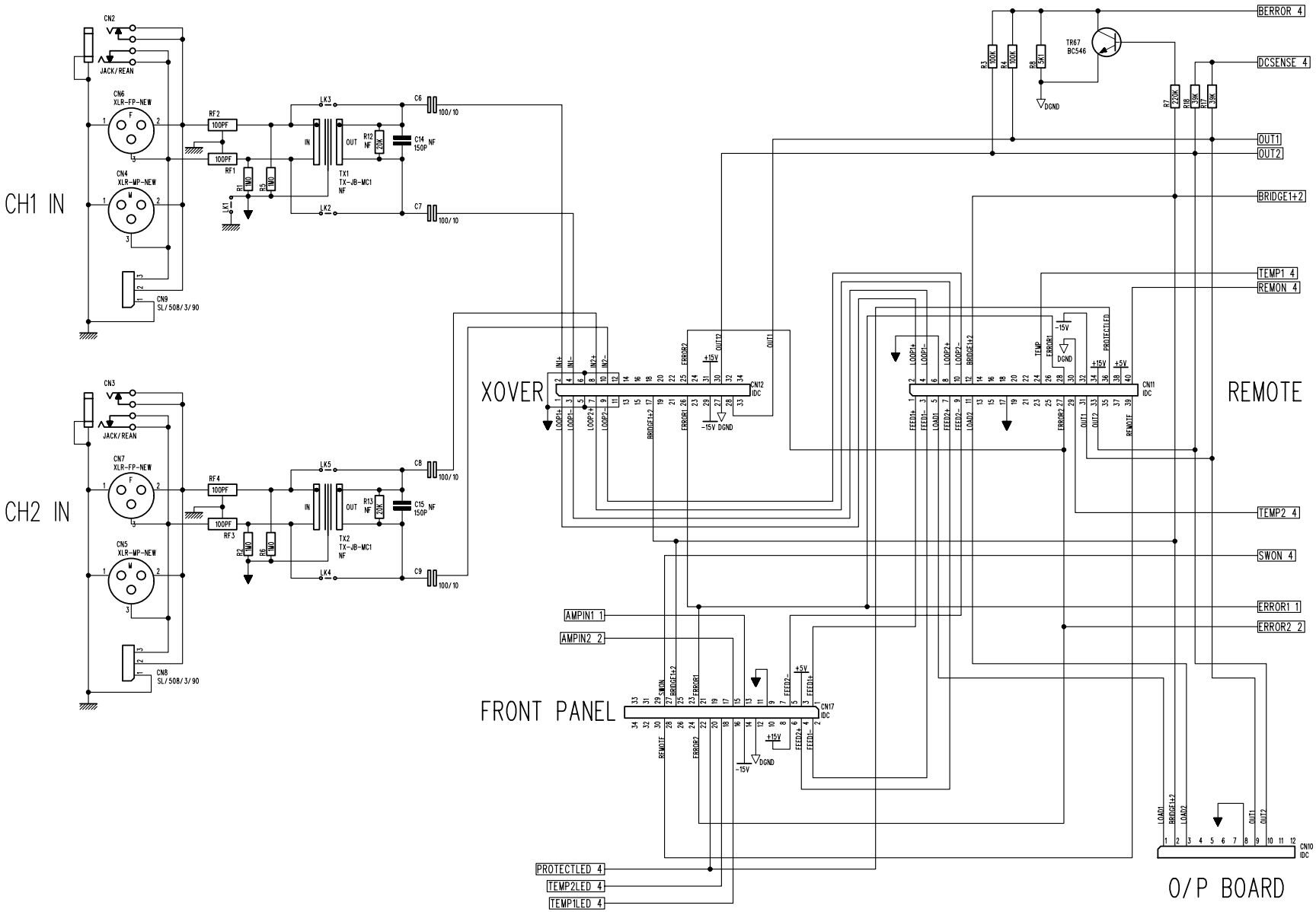
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRE-PRODUCTION RELEASE 10-05-99
2. PRODUCTION RELEASE 22-06-99
2A. ECN203 02/09/99
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
3. ECN0334 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C650AS-03

HARMAN INTERNATIONAL INDUSTRIES LIMITED
CRANBORNE HOUSE
CRANBORNE ROAD
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HERTS
EN6 3JN
Tel 01707 660667
Fax 01707 660755

TITLE: PULSE 2x650 AMPLIFIER

SHEET 4

FILENAME:

DRAWN: BPV

DATE: 04/01/00

CHECKED:

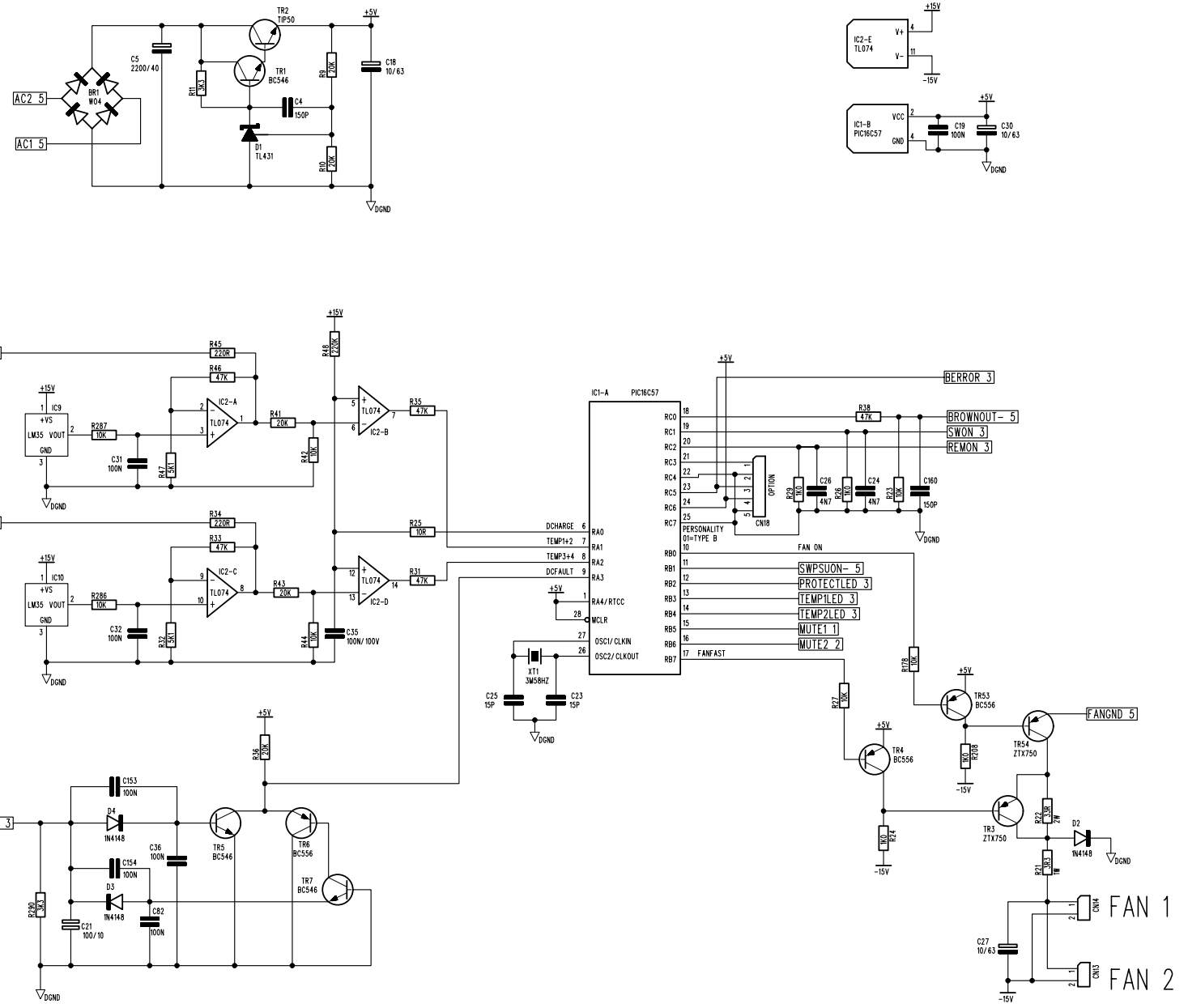
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRE-PRODUCTION RELEASE 10-05-99
2. PRODUCTION RELEASE 22-06-99
2A. ECN203 02/09/99
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
3. ECN0334 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C650AS-03

HARMAN INTERNATIONAL
INDUSTRIES LIMITED
CRANBORNE HOUSE
CRANBORNE ROAD
POTTERS BAR
HERTS
EN6 3JN
Tel 01707 660667
Fax 01707 660755

TITLE: PULSE 2x650 AMPLIFIER

SHEET 5

FILENAME:

DRAWN: BPV

DATE: 04/01/00

CHECKED:

MATERIAL:

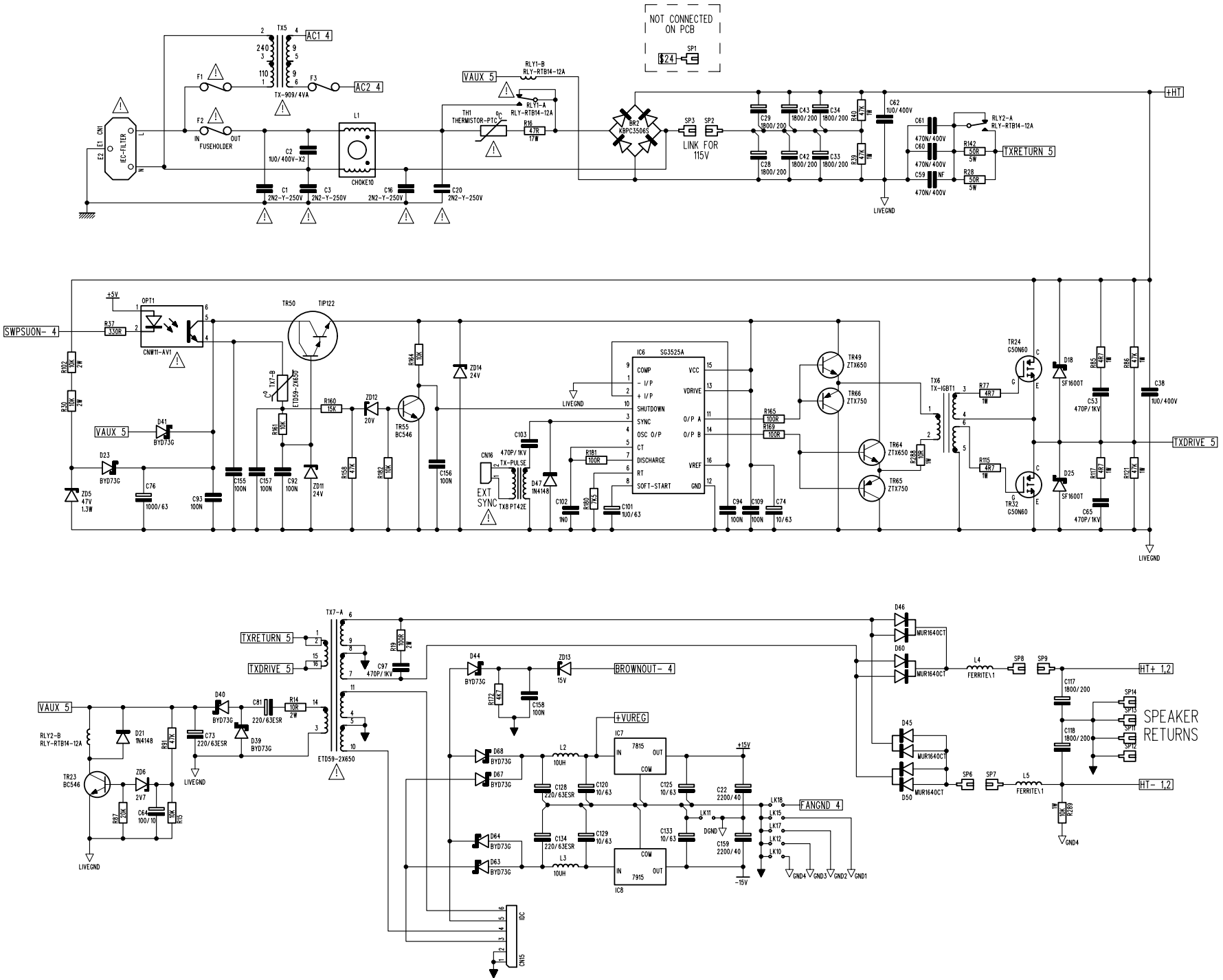
FINISH:

ISSUE COMMENTS:

1. PRE-PRODUCTION RELEASE 10-05-99
2. PRODUCTION RELEASE 22-06-99

2A. ECN203 02/09/99
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
3. ECN0334 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C650BS-02B

HARMAN INTERNATIONAL
INDUSTRIES LIMITED
CRANBORNE HOUSE
CRANBORNE ROAD
POTTERS BAR
HERTS
EN6 3JN
Tel 01707 660667
Fax 01707 660755

TITLE: PULSE 2X650 & 2X1100
SHEET 1 OF 1 FRONT PANEL

FILENAME:

DRAWN: BPV

DATE: 09-02-99

CHECKED:

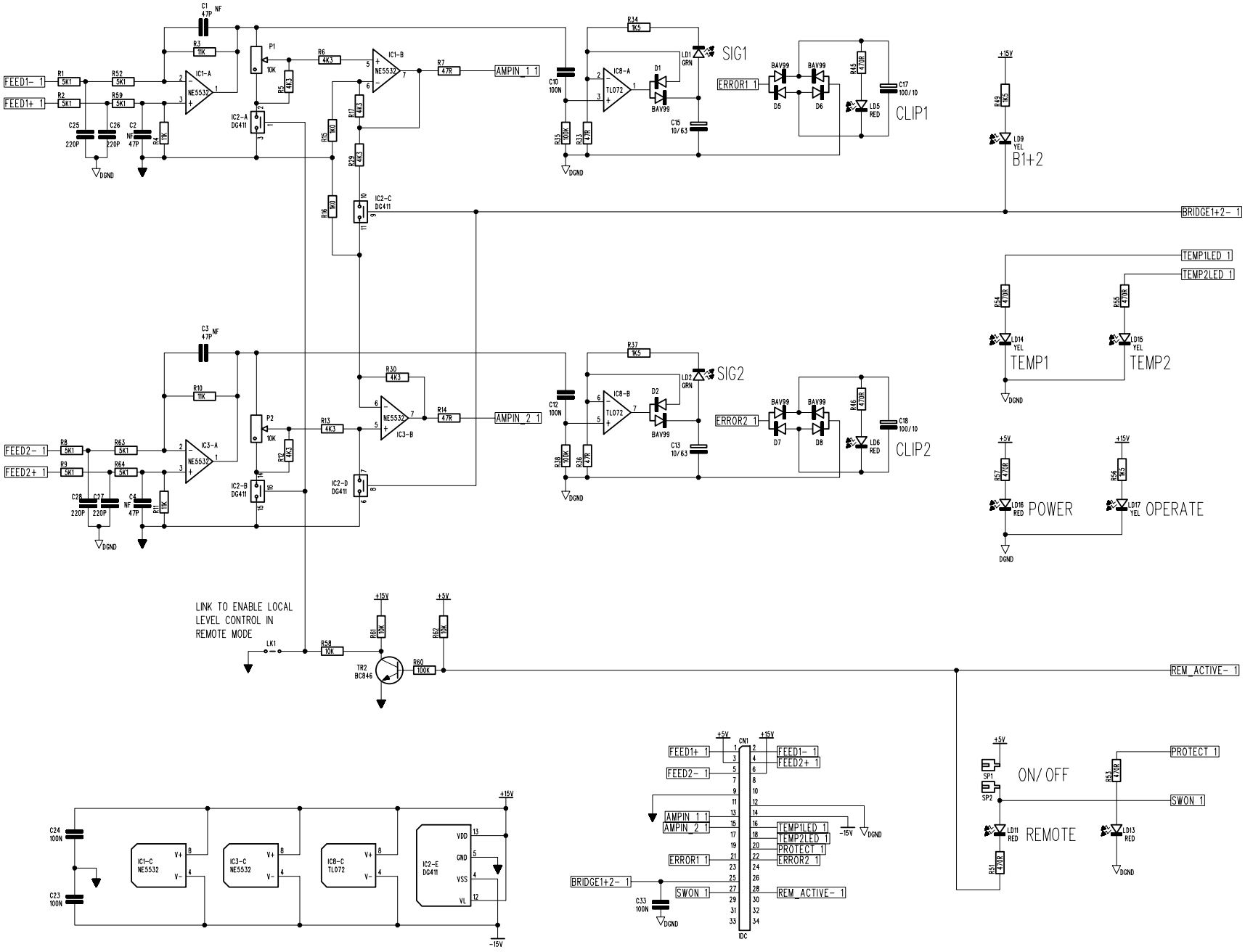
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRE-PRODUCTION RELEASE 10-05-99
2. PRODUCTION RELEASE 22-06-99
2A. ECN204 02/09/99
2B. ECN0330 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C1100AS-03

HARMAN INTERNATIONAL
INDUSTRIES LIMITED
CRANBORNE HOUSE
CRANBORNE ROAD
POTTERS BAR
HERTS
EN6 3JN
Tel 01707 660667
Fax 01707 660755

TITLE:
PULSE 2x1100
SHEET 1

FILENAME: S-C1100AS-03.SCH

DRAWN: BPV

DATE: 8/11/1999

CHECKED:

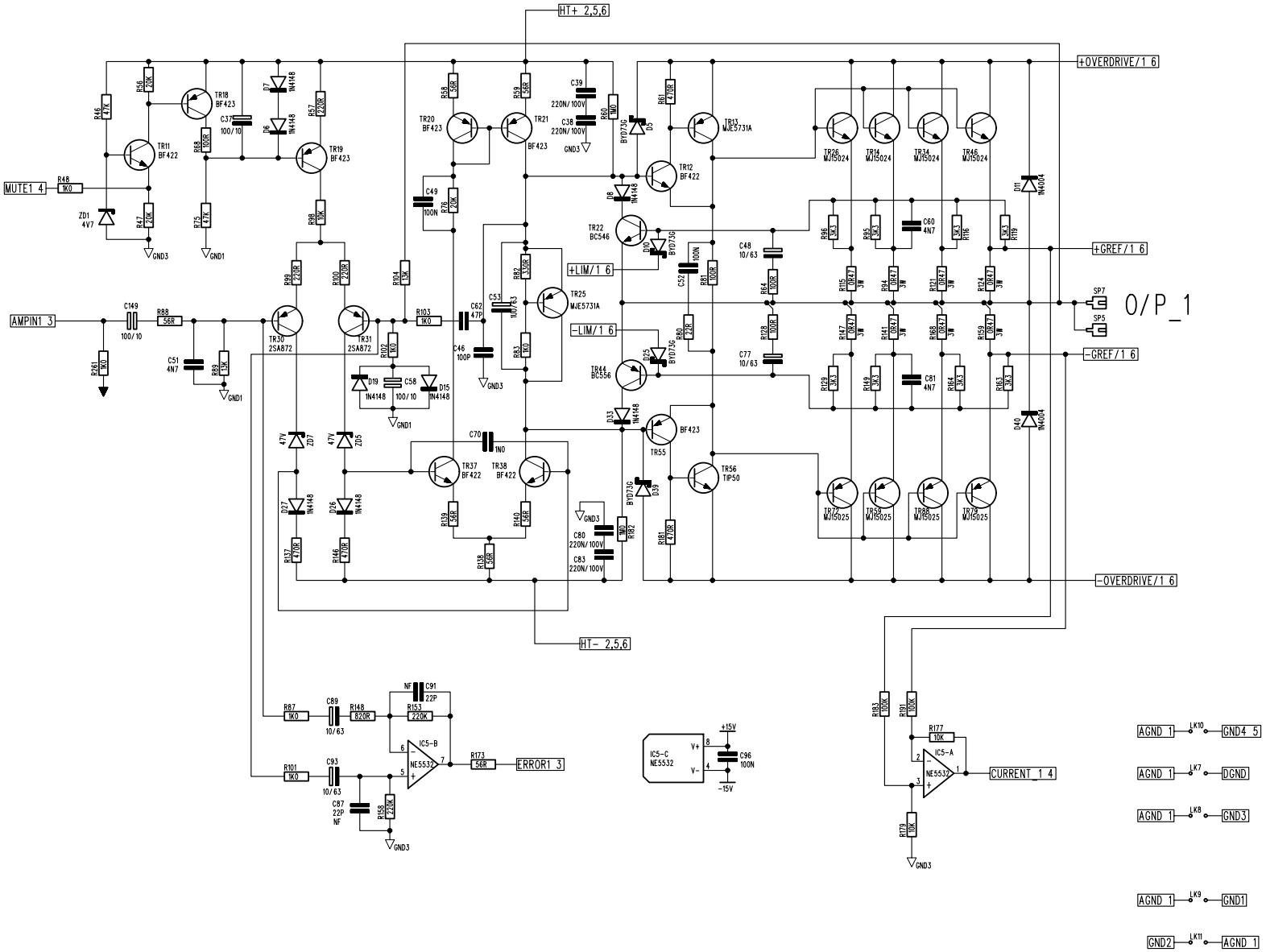
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PROTOTYPE
2. PRE-PRODUCTION ISSUE
2A. ECN0231 TX5 SYMBOL CORRECTED
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
2D. ECN0305 02/03/00
3. ECN0335 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C1100AS-03

HARMAN INTERNATIONAL
INDUSTRIES LIMITED
CRANBORNE HOUSE
CRANBORNE ROAD
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Fax 01707 660755

TITLE:

PULSE 2x1100

SHEET 2

FILENAME: S-C1100AS-03.SCH

DRAWN: BPV

DATE: 8/11/1999

CHECKED:

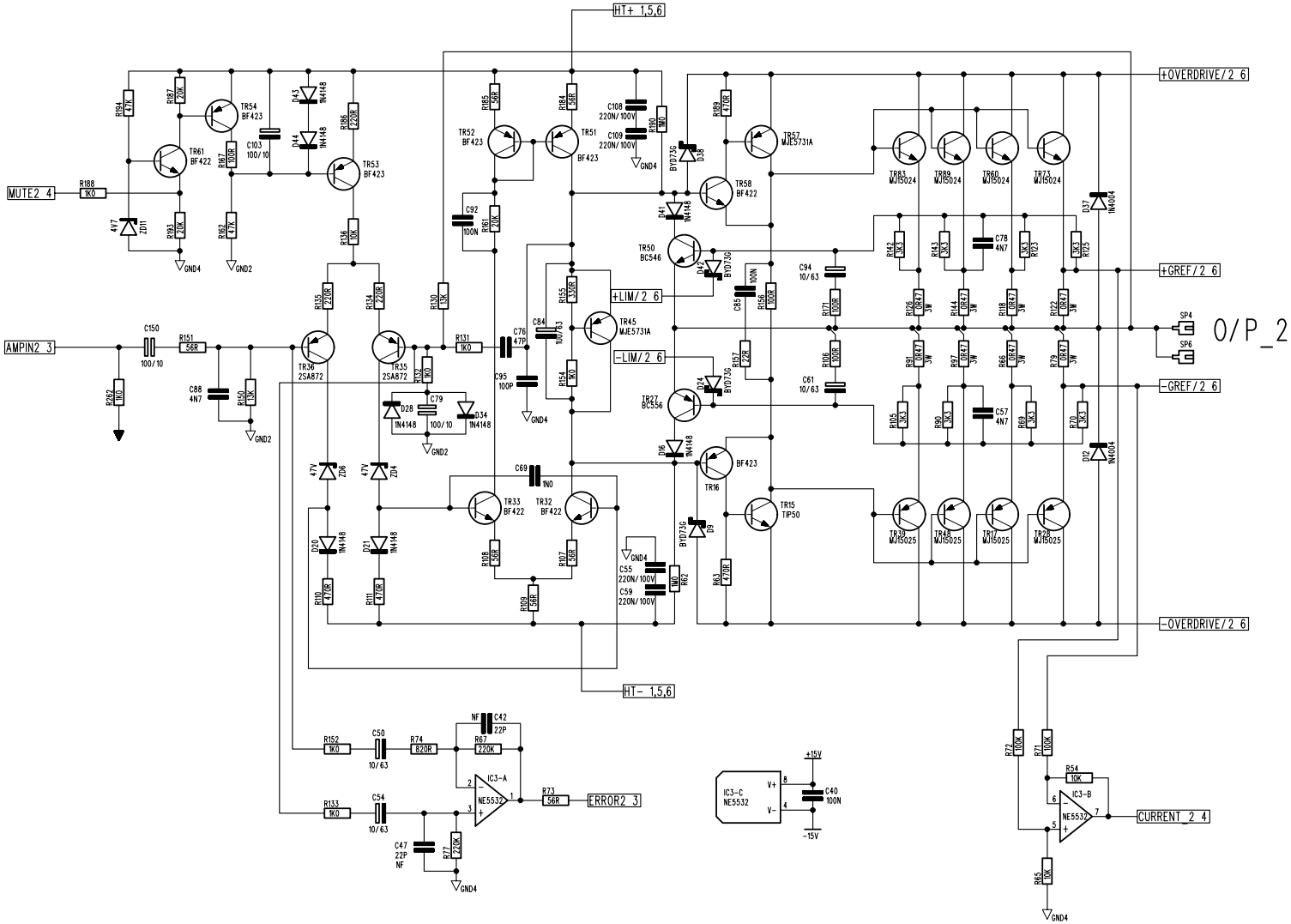
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PROTOTYPE
2. PRE-PRODUCTION ISSUE
2A. ECN0231 TX5 SYMBOL CORRECTED
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
2D. ECN0305 02/03/00
3. ECN0335 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C1100AS-03

HARMAN INTERNATIONAL
INDUSTRIES LIMITED
CRANBORNE HOUSE
CRANBORNE ROAD
POTTERS BAR
HERTS
EN6 3JN
Tel 01707 660667
Fax 01707 660755

TITLE:
PULSE 2x1100
SHEET 3

FILENAME: S-C1100AS-03.SCH

DRAWN: BPV

DATE: 8/11/1999

CHECKED:

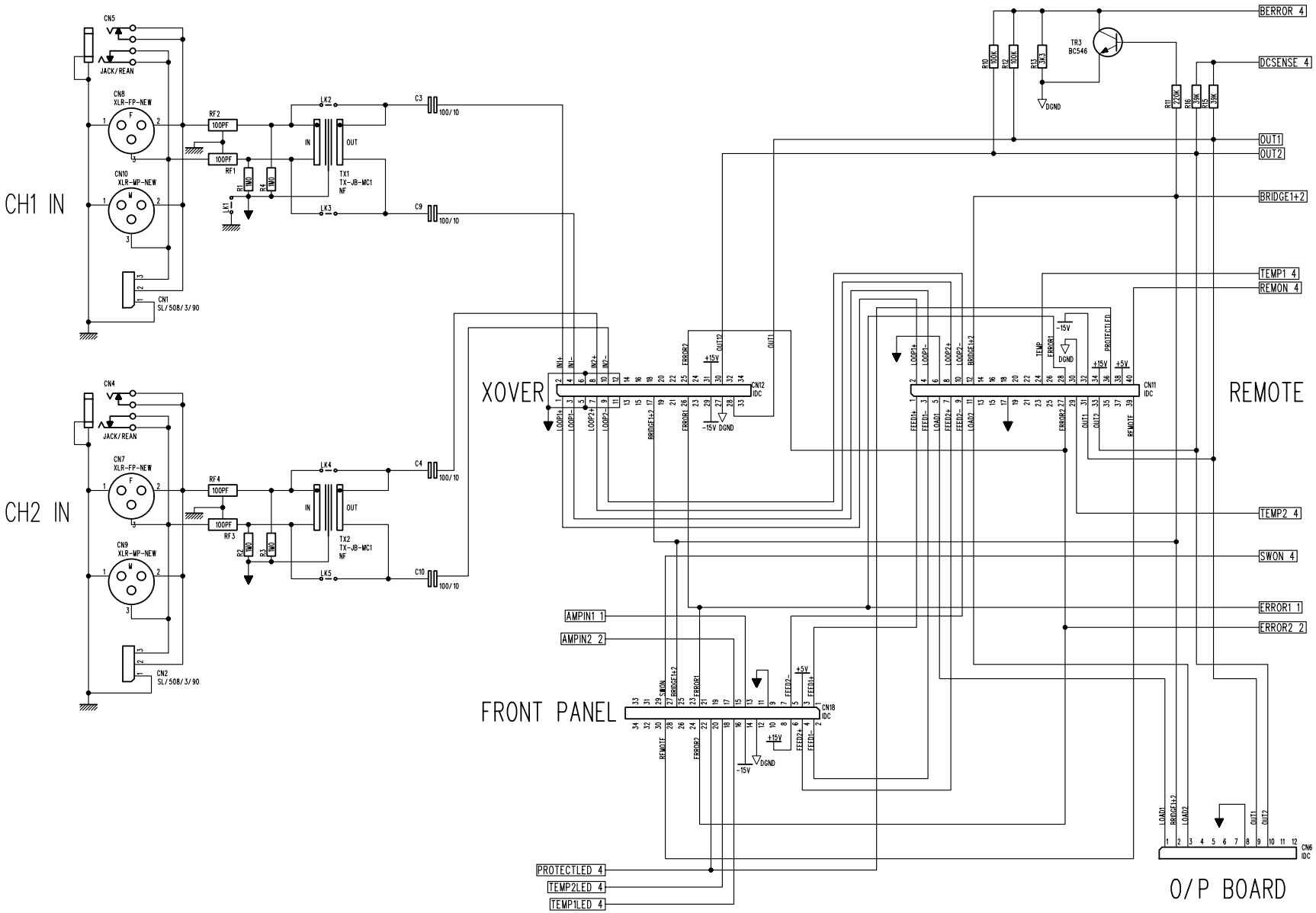
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PROTOTYPE
2. PRE-PRODUCTION ISSUE
2A. ECN0231 TX5 SYMBOL CORRECTED
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
2D. ECN0305 02/03/00
3. ECN0335 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C1100AS-03

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INDUSTRIES LIMITED
CRANBORNE HOUSE
CRANBORNE ROAD
POTTERS BAR
HERTS
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TITLE:
PULSE 2x1100
SHEET 4

FILENAME: S-C1100AS-03.SCH

DRAWN: BPV

DATE: 8/11/1999

CHECKED:

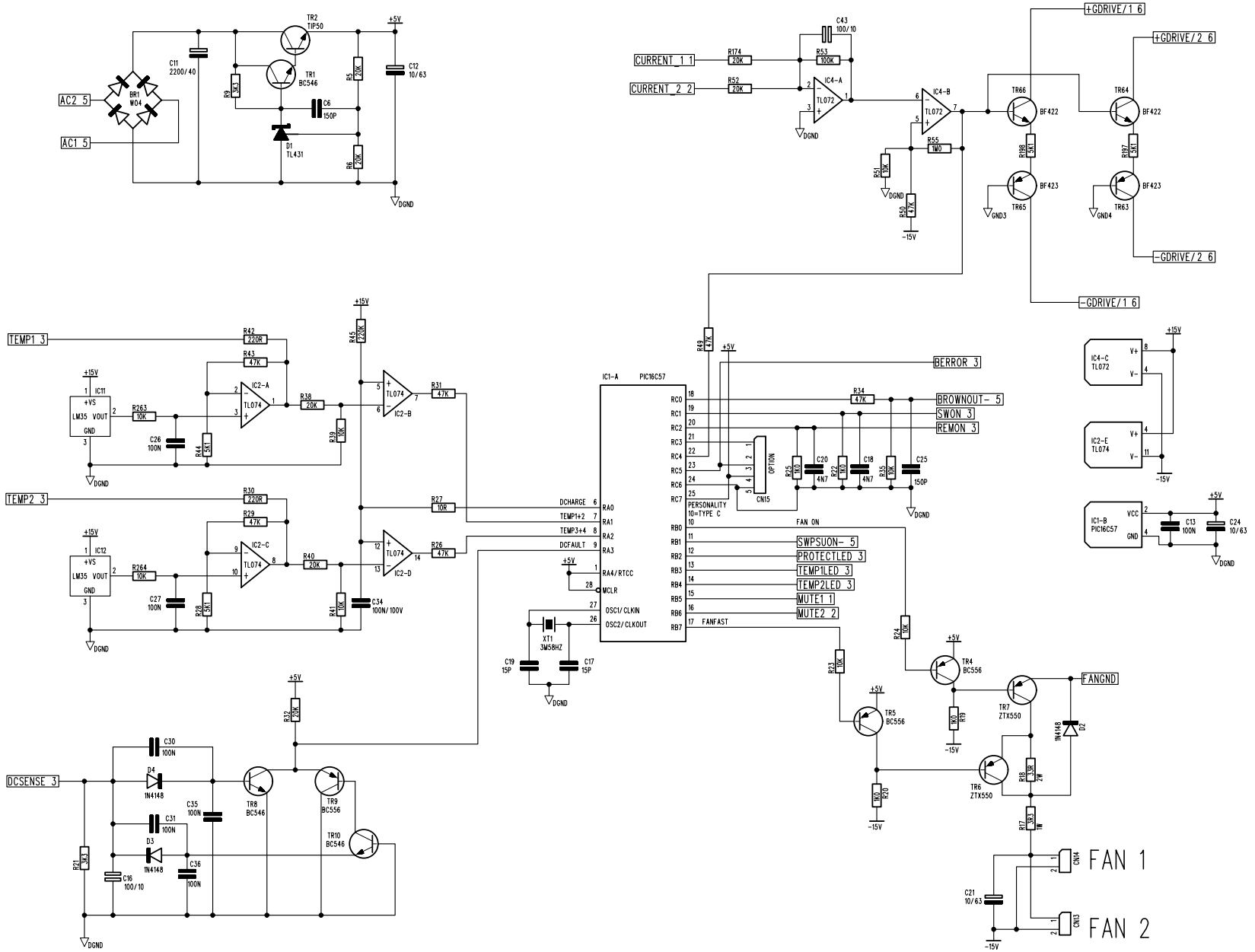
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PROTOTYPE
2. PRE-PRODUCTION ISSUE
2A. ECN0231 TX5 SYMBOL CORRECTED
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
2D. ECN0305 02/03/00
3. ECN0335 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C1100AS-03

HARMAN INTERNATIONAL
INDUSTRIES LIMITED
CRANBORNE HOUSE
CRANBORNE ROAD
POTTERS BAR
HERTS
EN6 3JN
Tel 01707 660667
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TITLE: PULSE 2x1100

SHEET 5

FILENAME: S-C1100AS-03.SCH

DRAWN: BPV

DATE: 8/11/1999

CHECKED:

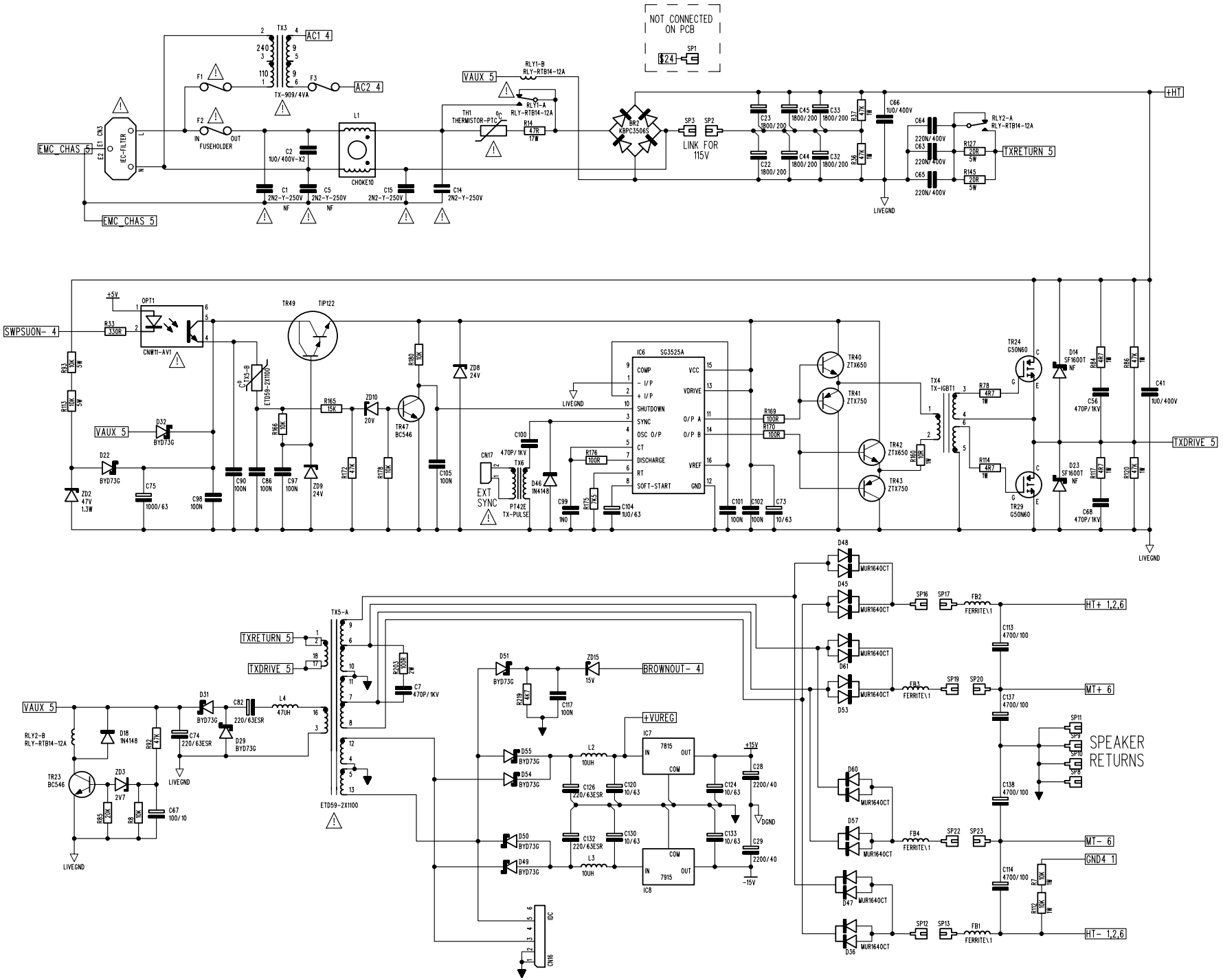
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PROTOTYPE
2. PRE-PRODUCTION ISSUE
2A. ECN0231 TX5 SYMBOL CORRECTED
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
2D. ECN0305 02/03/00
3. ECN0335 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C1100AS-03

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TITLE:
PULSE 2x1100
SHEET 6

FILENAME: S-C1100AS-03.SCH

DRAWN: BPV

DATE: 8/11/1999

CHECKED:

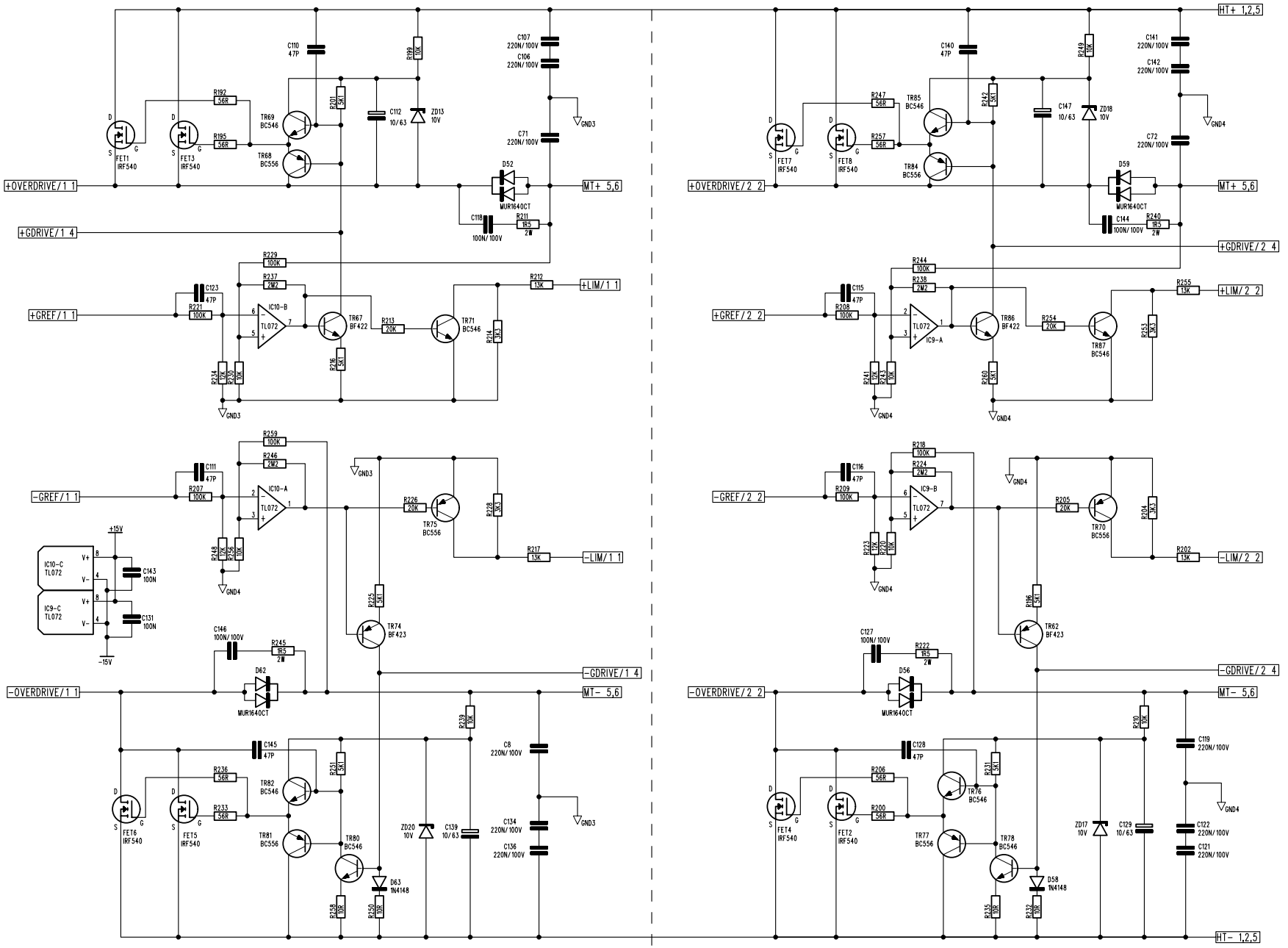
MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PROTOTYPE
2. PRE-PRODUCTION ISSUE
2A. ECN0231 TX5 SYMBOL CORRECTED
2B. ECN0251 15/11/99
2C. ECN0275 11/01/00
2D. ECN0305 02/03/00
3. ECN0335 05/05/00

PART NUMBER:



DRAWING NUMBER ISSUE

S-C208AS-01

audio

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TITLE: PULSE XOVER CARD

SHEET 1 OF 1

FILENAME: S-C208AS-01.SCH

DRAWN: BPV

DATE: 01-12-99

CHECKED:

MATERIAL:

FINISH:

ISSUE COMMENTS:

1. PRODUCTION RELEASE 01-12-99
A. R35,41,50,57 MADE 'NF'

DRAWING No WAS C208A-1A.