FORMENTI

F 19 SERVICE MANUAL

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CREATED BY E.G.

There are two different types of **F19** chassis that are equipped with two different microcontroller.

These microcontroller are known as ETT having a code SAA5297A and PAINTER with a code number SAA5553.

From the point of view of the application on the F19 chassis the two type of microcontroller are substantially having the same performances, the same pin-out , the same firmware but they are not interchangeable as the power supply are different.

In case of SAA5297A the power supply is 5 V for the SAA5553 is 3.3 V.

Even if the two devices are non interchangeable the two chassis can be interchanged as the in/out interface are exactly the same.

As the specifications of the two devices are the same and the first version of the chassis was equipped with the SAA5297A , in this document the characteristics of it are very much detailed meanwhile there is a very short description (as an addendum at the end) for the SAA5553.

F19 CHASSIS DESCRIPTION

Summary

The **F19** is a chassis suitable to drive CRT having both 4 by 3 and 16 to 9 aspect ratio and dimension from 25" up to 34".

As we can see from the block diagram the chassis is equipped with the most recent Integrated Circuit like the one chip TV processor TDA884x that does include all the low level signal processing including Video, Audio, synchronisation process, and chroma decoder . (see more detail at the "TDA884x FAMILY SPECIFICATION" paragraph), and the Sound Processor TDA9875A that perform all sound function including digital decoding of NICAM signals. (see more detail at the " TDA9870A & tda9875A MAIN CHARACTERISTICS" paragraph).

The above mentioned devices are driven by an Integrated Circuit that does include the microcontroller function with 64 K ROM and the TELETEXT acquisition and 8 pages RAM. (SAA5297A)

In the **F19** chassis there are, besides the stereo one, two possible module that are performing "FEATURES" like PIP (picture in picture) and / or CTI (colour transients improvement) and 4 by 3 to 16 by 9 signal processing. One further module is dedicated to the so called "Zero Power Stand By"

A 26 Key Remote Control is performing the full control for the end- used but can also be used in " SERVICE MODE" to control and adjust, without open the back cover of the TV set all the necessary functions.

With the 5 "LOCAL KEY BOARD" button all the end user function can also be performed

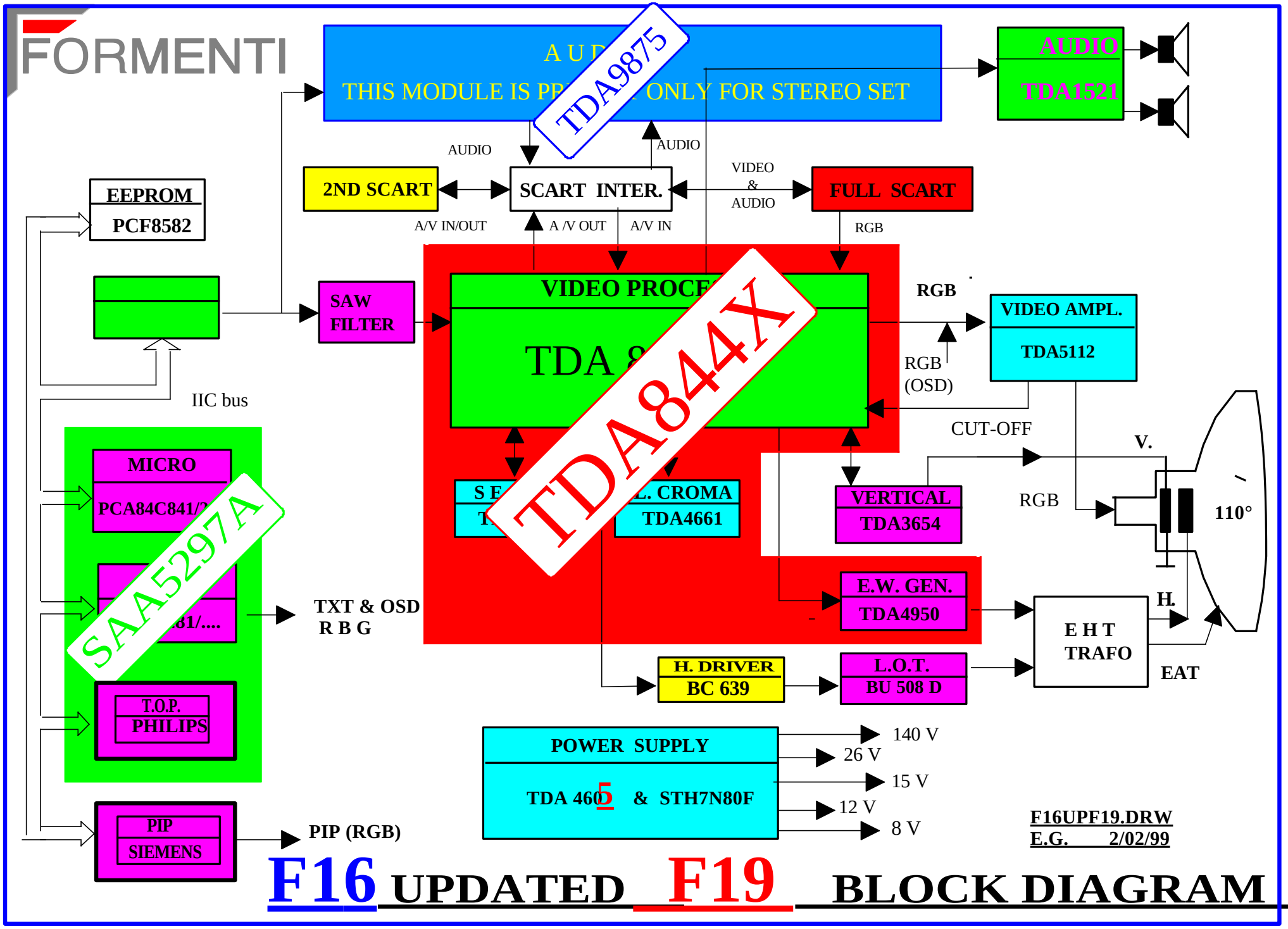
When the TV set is equipped with a PLL tuner the microcontroller recognise it and the tuning method became a frequency synthesis system if not it work as a voltage tuning system (provided all necessary components are mounted)

The TV make use of a multilevel MENU (activated both by the Remote Control and Local Keyboard) using five selectable languages (Italian, German, English, France, end Spanish) with which it is possible to control sequentially all video and sound value, to adjust several parameter like picture format, sound response, sleep timer etc., and to set others important parameter like standard, select country for automatic tuning and sort etc.

Here below a list of the characteristics of the TV se

TV SET CHARACTERISTICS (MONO & STEREO)

PICTURE TUBE SIZE :	
• 4 : 3 ASPECT RATIO	21" / 25" / 28" / 29" / 34"
• 16 : 9 ASPECT RATIO	28 " / 32"
• **STANDARD**	
• R.F. (ANTENNA) (FOR FREQ. SYNTH.)	CCIR (B / G/ L / L' / D / K / I)
• VIDEO (SCART & CINCH)	B / G/ L / L' / D / K / I / M / N
• COLOUR (MAX. THREE STANDARDS)	PAL / SECAM / NTSC
• SOUND STANDARD:	B / G/ L / L' / D / K / I
* MONO	AM & FM
* STEREO	A2 OR NICAM
TUNING SYSTEM SELECTABLE :	FACTORY OPTION
FREQUENCY SYTHETIZER	
• TOTAL AVAILABLE CHANNEL NUMBER	200
• CHANNEL IN ONE RF STANDARD UP TO	100
• NUMBER OF PROGRAM	100
• DIRECT PROGRAM & CHANNEL CALL WITH	1, OR 2 OR 3 DIGIT
• PROGRAM & CHANNEL STEP UP AND DOWN	YES
• VOLTAGE SYNTHESISER	
• CABLE & HYPERBAND CHANNEL	YES
• SWITCHABLE AFC	YES
• AUTOMATIC SEARCH TUNING	YES
• A S T WITH AUTO SORT	YES
AUDIO SECTION	
POWER	
• MONO	6 W RMS.
• STEREO	2 x 6 W RMS.
EXTERNAL CONNECTION	
• HEADPHONE	STEREO SET ONLY
• LOUDSPEAKERS	INTERNAL L.S. SWITCHED
A / V INPUT / OUTPUT	
• FRONT PANEL CINCH	A / V INPUT
• I FULL SCART (CVBS, STEREO, RBA)	MULTIMEDIA INPUT OUTPUT
• SCART (CVBS & STEREO IN / OUT)	VCR, HI.FI, SATELLITE, ETC
• SCART A TO SCART B LOOP THROUGH	FOR PROGRAMS DUBBING
TXT	PANEUROPEAN CHARACTER SET
• LEVEL 1	**8** PAGES
• LEVEL 1,5 (FASTEXT)	**7** PAGES
FEATURES	
• **CTI** (COLOUR TRANSIENT IMPROVEMENT)	**OPTION**
• **16:9 TO 4:3** VIDEO COMPRESSION	ONLY FOR 16:9 TV SET
• VERTICAL ZOOM OUT	3 LEVEL
• **MENU** DRIVEN SYSTEM	
• **EASY** TO USE REMOTE CONTROL	
• REMOTE CONTROL WITH "SERVICE" USE	NOT ACCESSIBLE TO END USER
• **PIP**	**OPTION**



F16 UPDATED F19 BLOCK DIAGRAM

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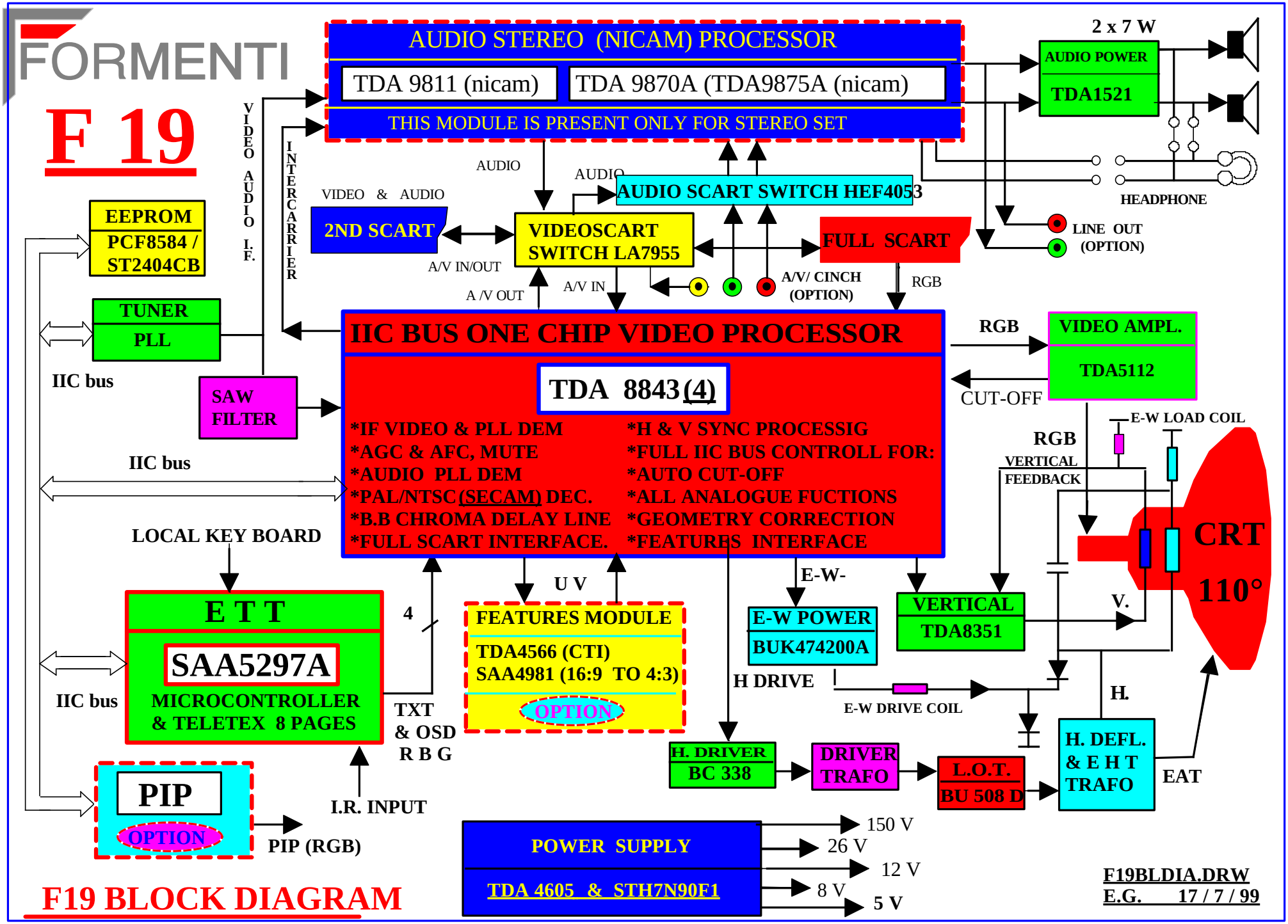
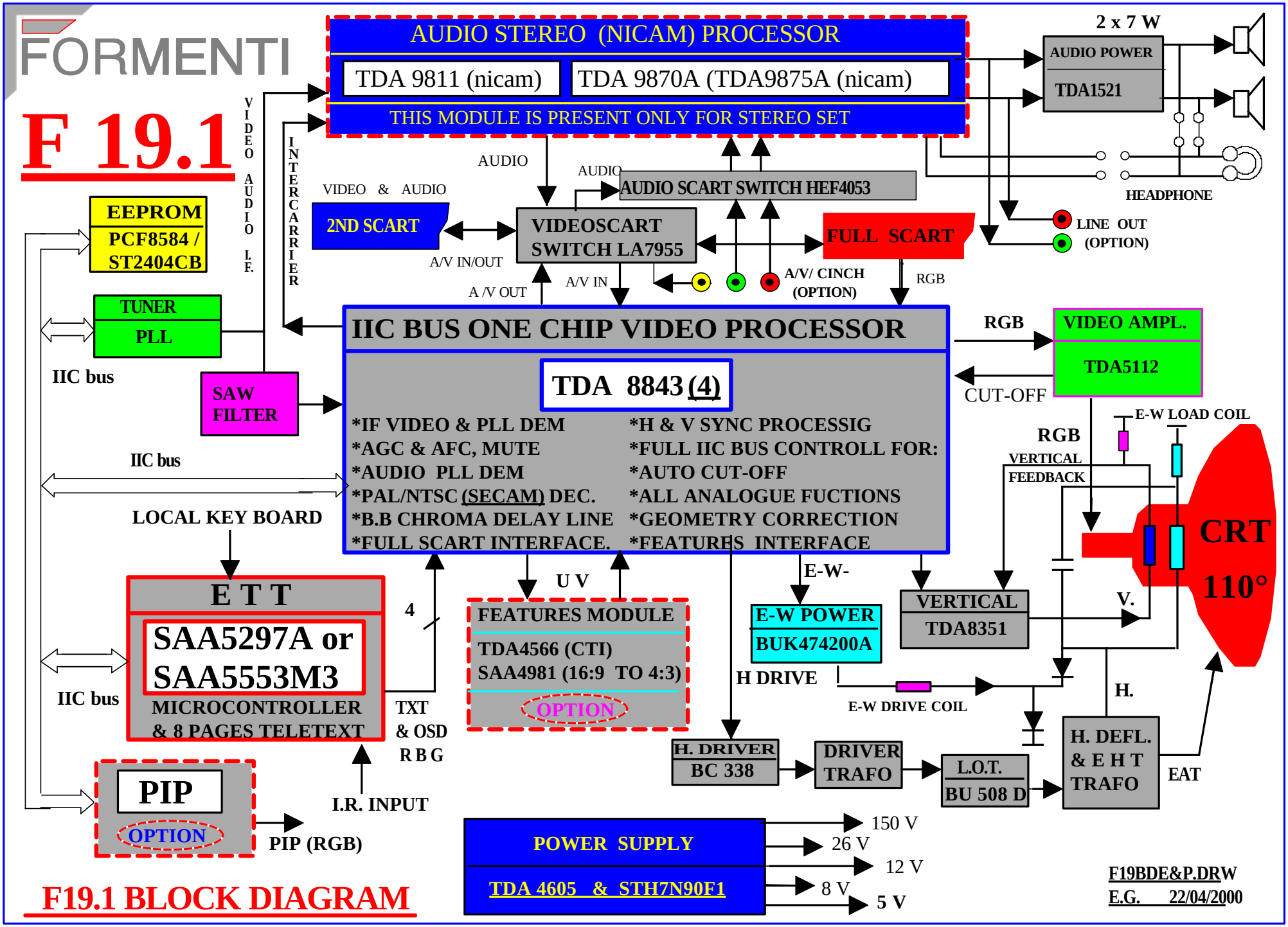
F 19



F19 BLOCK DIAGRAM

F19BLDIA.DRW
E.G. 17 / 7 / 99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F 19.1
AUDIO STEREO (NICAM) PROCESSOR
TDA 9811 (nicam)
TDA 9870A (TDA9875A (nicam)
THIS MODULE IS PRESENT ONLY FOR STEREO SET
2 x 7 W
AUDIO POWER
TDA1521
HEADPHONE
LINE OUT
(OPTION)
VIDEO AUDIO I.F.
INTERCARRIER
AUDIO
AUDIO
AUDIO SCART SWITCH HEF4053
VIDEO & AUDIO
2ND SCART
VIDEOSCART
SWITCH LA7955
FULL SCART
A/V IN/OUT
A /V OUT
A/V IN
A/V/ CINCH
(OPTION)
RGB
EEPROM
PCF8584 /
ST2404CB
TUNER
PLL
IIC bus
SAW
FILTER
IIC BUS ONE CHIP VIDEO PROCESSOR
TDA 8843 (4)
*IF VIDEO & PLL DEM
*AGC & AFC, MUTE
*AUDIO PLL DEM
*PAL/NTSC (SECAM) DEC.
*B.B CHROMA DELAY LINE
*FULL SCART INTERFACE.
*H & V SYNC PROCESSIG
*FULL IIC BUS CONTROLL FOR:
*AUTO CUT-OFF
*ALL ANALOGUE FUCTIONS
*GEOMETRY CORRECTION
*FEATURES INTERFACE
RGB
VIDEO AMPL.
TDA5112
CUT-OFF
E-W LOAD COIL
RGB
VERTICAL
FEEDBACK
IIC bus
LOCAL KEY BOARD
E T T
SAA5297A or
SAA5553M3
MICROCONTROLLER
& 8 PAGES TELETEXT
4
U V
FEATURES MODULE
TDA4566 (CTI)
SAA4981 (16:9 TO 4:3)
OPTION
E-W-
E-W POWER
BUK474200A
VERTICAL
TDA8351
V.
CRT
110°
H DRIVE
E-W DRIVE COIL
H.
IIC bus
TXT
& OSD
R B G
H. DRIVER
BC 338
DRIVER
TRAFO
L.O.T.
BU 508 D
H. DEFL.
& E H T
TRAFO
EAT
PIP
OPTION
I.R. INPUT
PIP (RGB)
POWER SUPPLY
TDA 4605 & STH7N90F1
150 V
26 V
12 V
8 V
5 V
F19BDE&P.DRW
E.G. 22/04/2000
F19.1 BLOCK DIAGRAM

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F19 TUNING

&

TELETEXT

SAA529XA FAMILY MAIN CHARACTERISTICS

FEATURES

General

- Single chip microcontroller with integrated teletext decoder
- Single +5 V power supply
- Single crystal oscillator for teletext decoder, display and microcontroller
- Teletext function can be powered-down independent of microcontroller function for reduced power consumption in standby
- Pin compatibility throughout family.

Microcontroller

- 80C51 microcontroller core
- 16/32/64 kbyte mask programmed ROM
- 256/768/1280 bytes of microcontroller RAM
- Eight 6-bit Pulse Width Modulator (PWM) outputs for control of TV analog signals
- One 14-bit PWM for Voltage Synthesis Tuner control
- Four 8-bit Analog-to-Digital converters
- 2 high current open-drain outputs for directly driving LEDs etc.
- I 2 C-bus interface
- External ROM and RAM capability on QFP80 package version.

Teletext acquisition

- 1 page and 10 page Teletext version
- Acquisition of 525-line and 625-line World System Teletext, with automatic selection
- Acquisition and decoding of VPS data (PDC system A)
- Page clearing in under 64 s (1 TV line)
- Separate storage of extension packets (SAA5296/7, SAA5296/7A and SAA5496/7)
- Inventory of transmitted Teletext pages stored in the Transmitted Page Table (TPT) end Subtitle Page Table (SPT) (SAA5296/7, SAA5296/7A and SAA5496/7)
- Automatic detection of FASTEXT transmission

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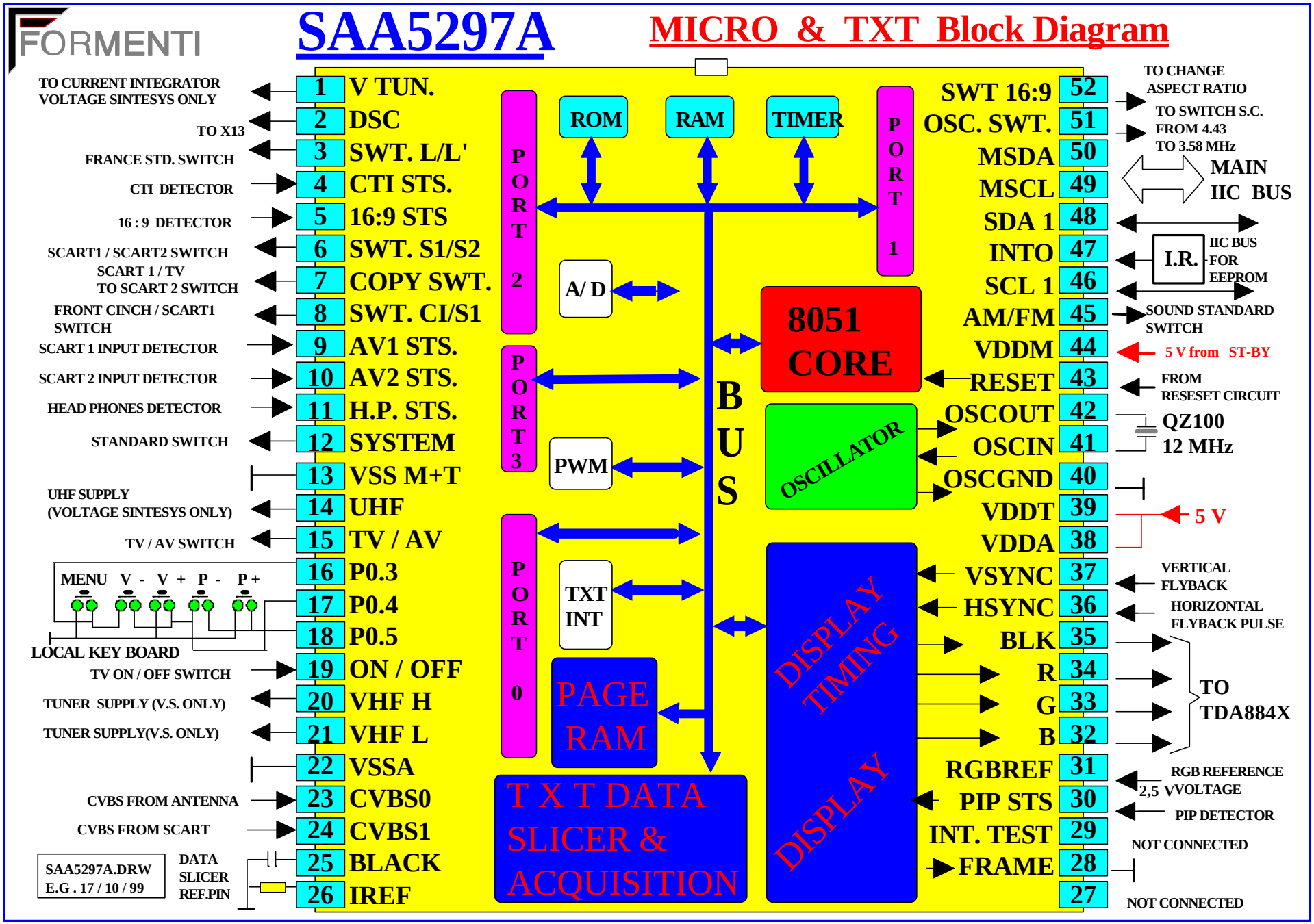
SAA5297A

MICRO & TXT Block Diagram



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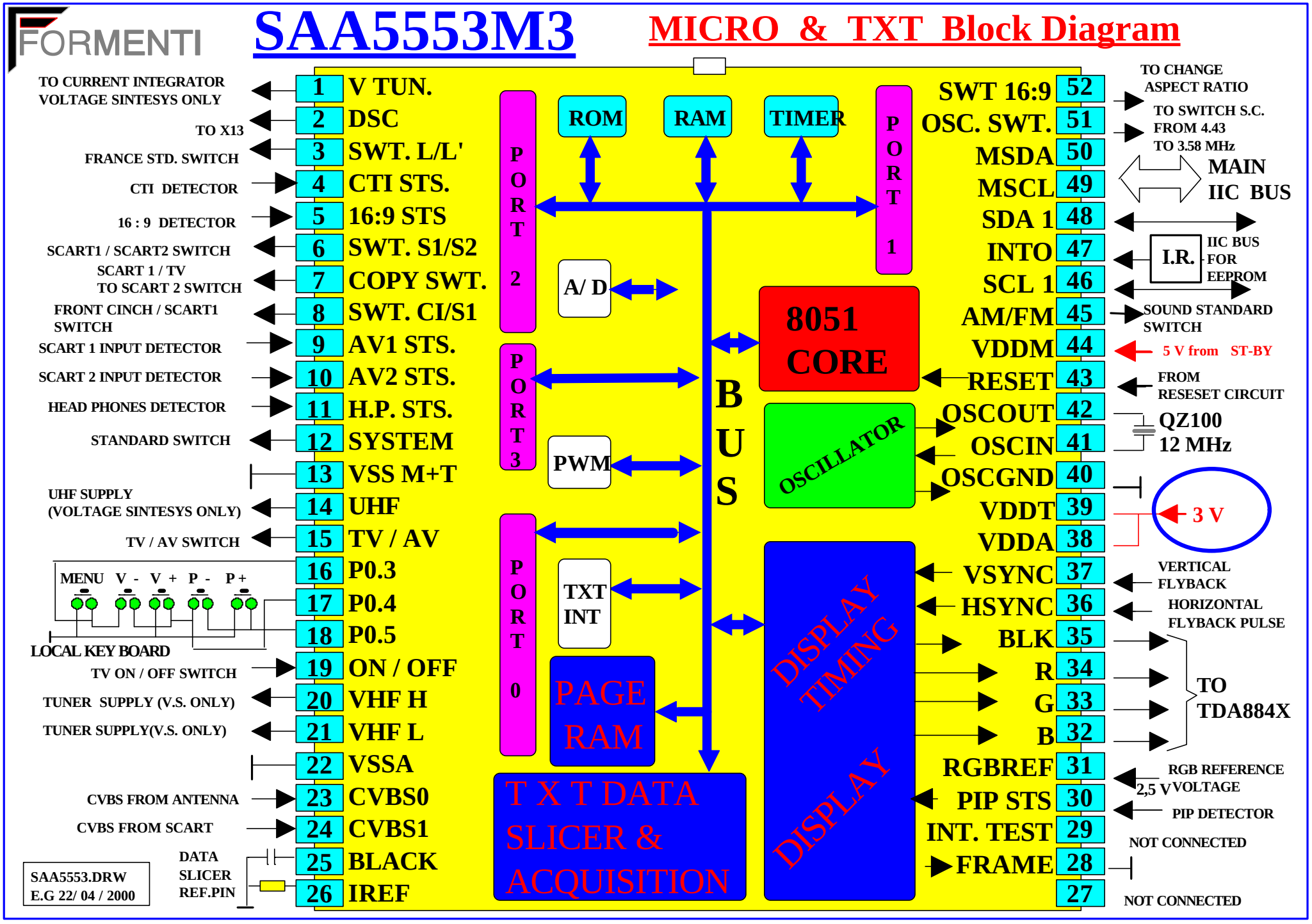
SAA5553M3

MICRO & TXT Block Diagram



- Real-time packet 26 engine for processing accented (and other) characters
- Comprehensive Teletext language coverage
- Video signal quality detector.

Teletext Display

- 525-line and 625-line display
- 12 10 character matrix
- Double height, width and size On-Screen Display (OSD)
- Definable border colour
- Enhanced display features including meshing and shadowing
- 260 characters in mask programmed ROM
- Automatic FRAME output control with manual override
- RGB push-pull output to standard decoder ICs
- Stable display via slave synchronisation to horizontal sync and vertical sync.

Additional features of SAA529xA devices

- Wide Screen Signalling (WSS) bit decoding (line 23).

2 GENERAL DESCRIPTION

The SAA529x, SAA529xA and SAA549x family of microcontrollers are a derivative of the Philips' industry-standard 80C51 microcontroller and are intended for use as the central control mechanism in a television receiver. They provide control functions for the television system and include an integrated teletext function.

The teletext hardware has the capability of decoding and displaying both 525-line and 625-line World System Teletext. The same display hardware is used both for Teletext and On-Screen Display, which means that the display features give greater flexibility to differentiate the TV set.

The family offers both 1 page and 10 page Teletext capability, in a range of ROM sizes. Increasing display capability is offered from the SAA5290 to the SAA5497.

TELETEXT DECODER

Data slicer

The data slicer extracts the digital teletext data from the incoming analog waveform. This is performed by sampling the CVBS waveform and processing the samples to extract the teletext data and clock.

Acquisition timing

The acquisition timing is generated from a logic level positive-going composite sync signal VCS. This signal is generated by a sync separator circuit which adaptively slices the sync pulses. The acquisition clocking and timing are locked to the VCS signal using a digital phase-locked-loop. The phase error in the acquisition phase-locked-loop is detected by a signal quality circuit which disables acquisition if poor signal quality is detected.

Teletext acquisition

This family is capable of acquiring 625-line and 525-line World System Teletext see “World System Teletext and Data Broadcasting System”. Teletext pages are identified by seven numbers: magazine (page hundreds), page tens, page units, hours tens, hours units, minutes tens and minutes units. The last four digits, hours and minutes, are known as the subcode, and were originally intended to be time related, hence their names.

For the ten page device, each packet can only be written into one place in the teletext RAM so if a page matches more than one of the page requests the data is written into the area of memory corresponding to the lowest numbered matching page request.

At power-up each page request defaults to any page, hold on and error check Mode 0.

Rolling headers and time

When a new page has been requested it is conventional for the decoder to turn the header row of the display green and to display each page header as it arrives until the correct page has been found.

Error checking

Before teletext packets are written into the page memory they are error checked. The error checking carried out depends on the packet number, the byte number, the error check mode bits in the page request data and the TXT1.8 BIT bit. If an uncorrectable error occurs in one of the Hamming checked addressing and control bytes in the page header or in the Hamming checked bytes in packet 8/30, bit 4 of the byte written into the memory is set, to act as an error flag to the software. If uncorrectable errors are detected in any other Hamming checked data the byte is not written into the memory.

Packet 26 processing

One of the uses of packet 26 is to transmit characters which are not in the basic teletext character set. The family automatically decodes packet 26 data and, if a character corresponding to that being transmitted is available in the character set, automatically writes the appropriate character code into the correct location in the teletext memory. This is not a full implementation of the packet 26 specification allowed for in level 2 teletext, and so is often referred to as level 1.5.

By convention, the packets 26 for a page are transmitted before the normal packets. To prevent the default character data overwriting the packet 26 data the device incorporates a mechanism which prevents packet 26 data from being overwritten.

Fastext detection

When a packet 27, designation code 0 is detected, whether or not it is acquired, the TXT13.FASTEXT bit is set. If the device is receiving 525-line teletext, a packet X/0/27/0 is required to set the flag. The flag can be reset by writing a logic 0 into the SFR bit.

When a packet 8/30 is detected, or a packet 4/30 when the device is receiving a 525-line transmission, the TXT13.Pkt 8/30 is set. The flag can be reset by writing a logic 0 into the SFR bit.

THE DISPLAY

Introduction

The capabilities of the display are based on the requirements of level 1 teletext, with some enhancements for use with locally generated on screen displays. The display consists of 25 rows each of 40 characters, with the characters displayed being those from rows 0 to 24 of the basic page memory. If the TXT7.STATUS ROW TOP bit is set row 24 is displayed at the top of the screen, followed by row 0, but normally memory rows are displayed in numerical order. The teletext memory stores 8 bit character codes which correspond to a number of displayable characters and control characters, which are normally displayed as spaces. The character set of the device is described in more detail below.

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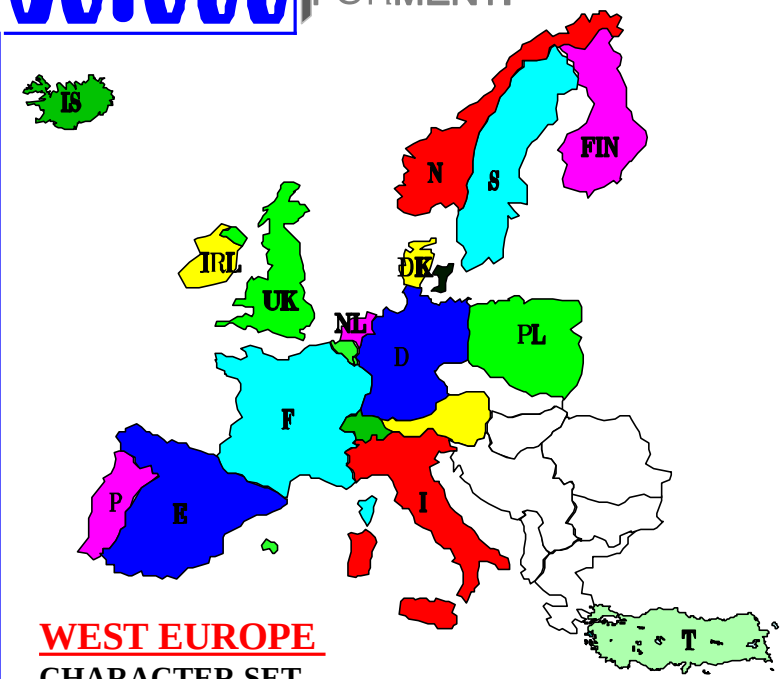


WEST EUROPE

CHARACTER SET
NATIONAL OPTION FOR:

ENGLISH
GERMAN
SWEDISH
ITALIAN
FREANCH
SPANISH
TURKISH

(OPTION BYTE 1 BIT 6 SETTED TO 1

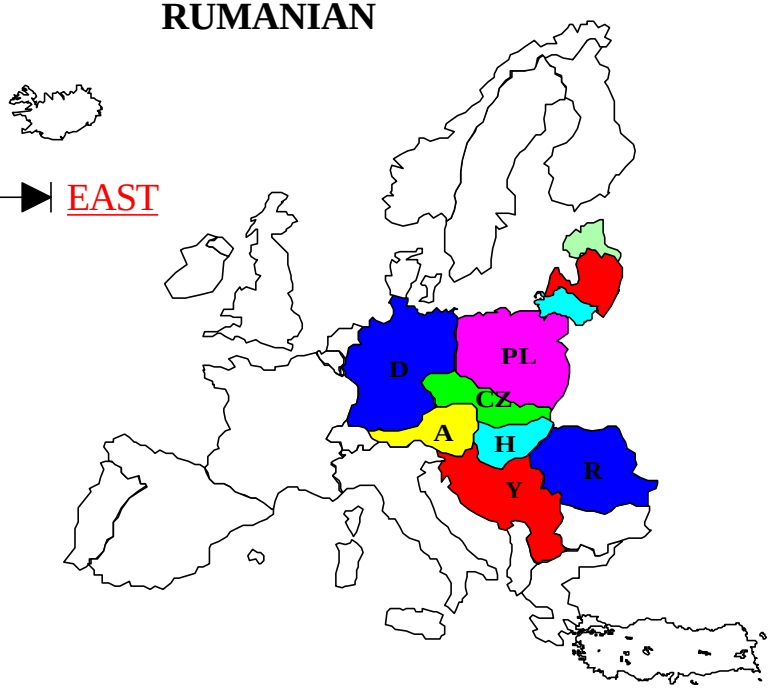
WEST ◄——► EAST

(OPTION BYTE 1 BIT 3 SETTED TO 0

EAST EUROPE

CHARACTER SET
NATIONAL OPTION FOR:

POLISH
GERMAN
ESTONIAN
SERBO-CROAT
CZECH
SLOVAKIA
RUMANIAN



F19 E&WCS.DRW
E.G. 7/11/99

Character matrix

Each character is defined by a matrix 12 pixels wide and 10 pixels high. When displayed, each pixel is 1 12 s wide and 1 TV line, in each field, high.

East/West selection

In common with their predecessors, these devices store teletext pages as a series of 8 bit character codes which are interpreted as either control codes (to change colour, invoke flashing etc.) or displayable characters. When the control characters are excluded, this gives an addressable set of 212 characters at any given time.

National option characters

The meanings of some character codes between 20H and 7FH depend on the C12 to C14 language control bits from the teletext page header.

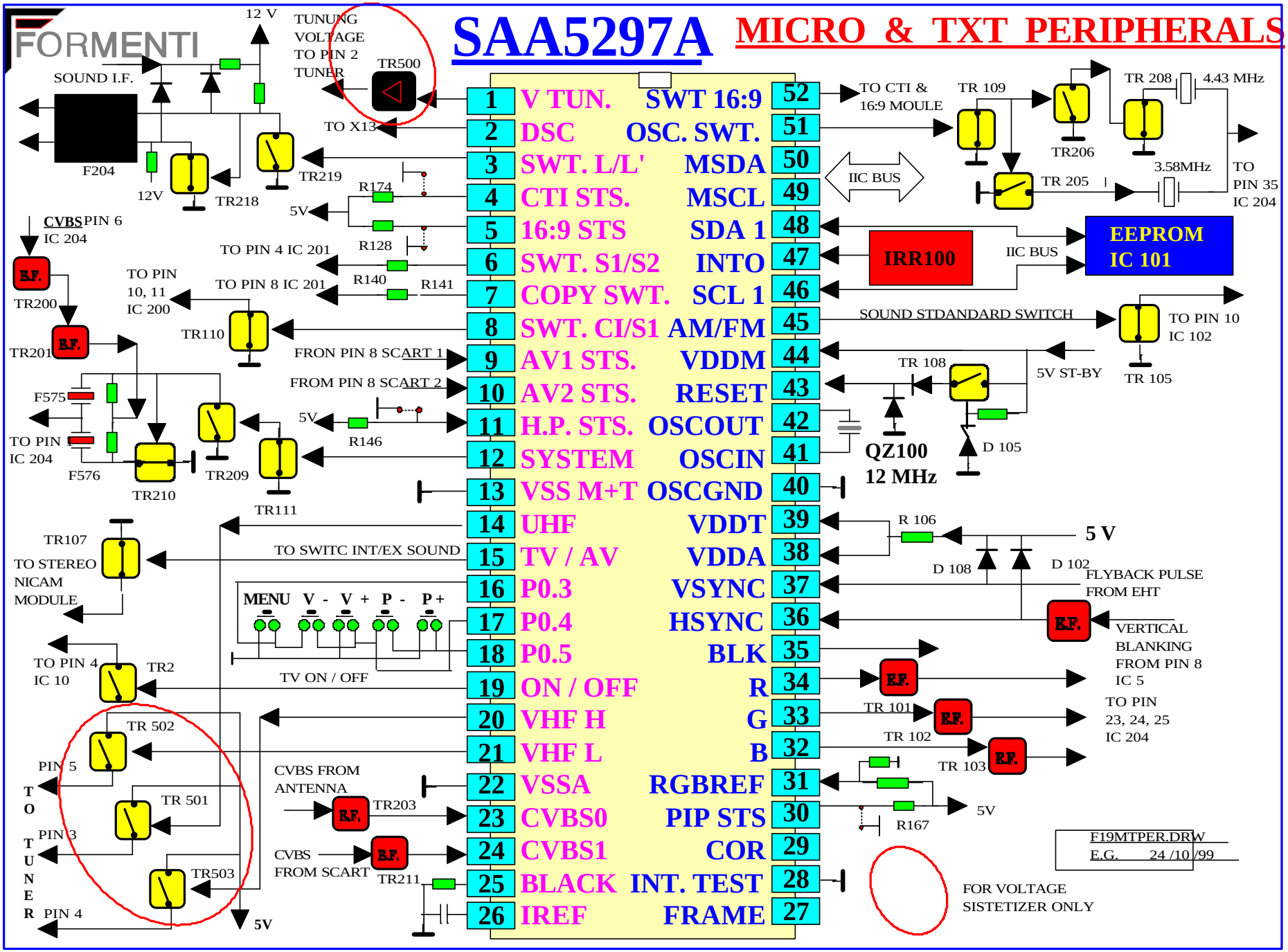
The interpretation of the C12 to C14 language control bits is dependent on the East/West bit.

On-Screen Display characters

Character codes 80H to 9FH are not addressed by the teletext decoding hardware. An editor is available to allow these characters to be redefined by the customer. The alternative character shapes in columns 8a and 9a (SAA549x only) can be displayed when the ‘graphics’ serial attribute is set. This increases the number of customer definable characters to 64.

Clock generator

The oscillator circuit is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between XTALIN and XTALOUT is basically an inverter biased to the transfer point. A crystal must be used as the feedback element to complete the oscillator circuitry. It is operated in parallel resonance. XTALIN is the high gain amplifier input and XTALOUT is the output. To drive the device externally XTALIN is driven from an external source and XTALOUT is left open-circuit.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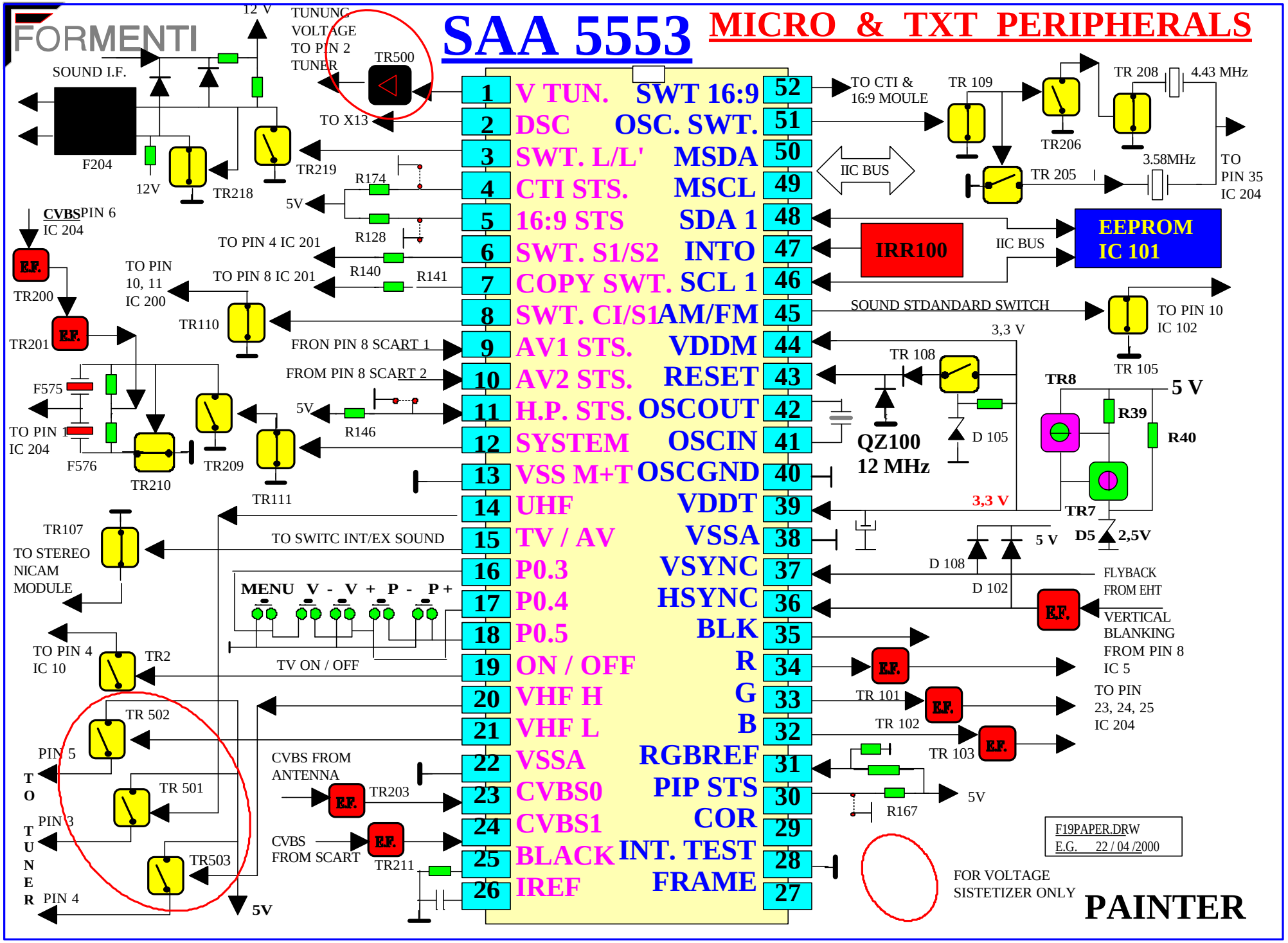
SAA5297A
MICRO & TXT PERIPHERALS
1 V TUN.
2 DSC
3 SWT. L/L'
4 CTI STS.
5 16:9 STS
6 SWT. S1/S2
7 COPY SWT.
8 SWT. CI/S1
9 AV1 STS.
10 AV2 STS.
11 H.P. STS.
12 SYSTEM
13 VSS M+T
14 UHF
15 TV / AV
16 P0.3
17 P0.4
18 P0.5
19 ON / OFF
20 VHF H
21 VHF L
22 VSSA
23 CVBS0
24 CVBS1
25 BLACK
26 IREF
52 SWT 16:9
51 OSC. SWT.
50 MSDA
49 MSCL
48 SDA 1
47 INTO
46 SCL 1
45 AM/FM
44 VDDM
43 RESET
42 OSCOUT
41 OSCIN
40 OSCGND
39 VDDT
38 VDDA
37 VSYNC
36 HSYNC
35 BLK
34 R
33 G
32 B
31 RGBREF
30 PIP STS
29 COR
28 INT. TEST
27 FRAME
12 V
TUNUNG VOLTAGE TO PIN 2 TUNER
TR500
TO X13
SOUND I.F.
F204
12V
TR218
TR219
5V
R174
R128
R140
R141
CVBS PIN 6 IC 204
TO PIN 4 IC 201
TO PIN 8 IC 201
TO PIN 10, 11 IC 200
TR110
TR200
TR201
F575
F576
TO PIN 1 IC 204
TR209
TR210
TR111
FRON PIN 8 SCART 1
FROM PIN 8 SCART 2
R146
TR107
TO STEREO NICAM MODULE
TO SWITC INT/EX SOUND
MENU V - V + P - P +
TV ON / OFF
TO PIN 4 IC 10
TR2
TR 502
TR 501
TR503
PIN 5
PIN 3
PIN 4
TO TUNER
5V
CVBS FROM ANTENNA
TR203
CVBS FROM SCART
TR211
TO CTI & 16:9 MOULE
IIC BUS
IRR100
EEPROM IC 101
TR 109
TR206
TR 208
4.43 MHz
TR 205
3.58MHz
TO PIN 35 IC 204
SOUND STDANDARD SWITCH
TO PIN 10 IC 102
TR 105
TR 108
5V ST-BY
D 105
QZ100 12 MHz
R 106
5 V
D 108
D 102
FLYBACK PULSE FROM EHT
VERTICAL BLANKING FROM PIN 8 IC 5
TR 101
TR 102
TR 103
TO PIN 23, 24, 25 IC 204
R167
F19MTPER.DRW
E.G. 24 /10 /99
FOR VOLTAGE SISTETIZER ONLY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SAA 5553
MICRO & TXT PERIPHERALS
SOUND I.F.
12 V
TUNUNG VOLTAGE TO PIN 2 TUNER
TR500
TO X13
F204
12V
TR218
TR219
5V
R174
R128
CVBSPIN 6 IC 204
E.F.
TR200
TR201
TO PIN 4 IC 201
TO PIN 8 IC 201
R140
R141
TO PIN 10, 11 IC 200
TR110
FRON PIN 8 SCART 1
FROM PIN 8 SCART 2
F575
F576
TO PIN 1 IC 204
TR210
TR209
TR111
5V
R146
TR107
TO STEREO NICAM MODULE
TO SWITC INT/EX SOUND
MENU V - V + P - P +
TV ON / OFF
TO PIN 4 IC 10
TR2
TR 502
TR 501
TR503
PIN 5
PIN 3
PIN 4
TO TUNER
5V
CVBS FROM ANTENNA
CVBS FROM SCART
TR203
TR211
1 V TUN.
2 DSC
3 SWT. L/L'
4 CTI STS.
5 16:9 STS
6 SWT. S1/S2
7 COPY SWT.
8 SWT. CI/S1
9 AV1 STS.
10 AV2 STS.
11 H.P. STS.
12 SYSTEM
13 VSS M+T
14 UHF
15 TV / AV
16 P0.3
17 P0.4
18 P0.5
19 ON / OFF
20 VHF H
21 VHF L
22 VSSA
23 CVBS0
24 CVBS1
25 BLACK
26 IREF
SWT 16:9 52
OSC. SWT. 51
MSDA 50
MSCL 49
SDA 1 48
INTO 47
SCL 1 46
AM/FM 45
VDDM 44
RESET 43
OSCOUT 42
OSCIN 41
OSCGND 40
VDDT 39
VSSA 38
VSYNC 37
HSYNC 36
BLK 35
R 34
G 33
B 32
RGBREF 31
PIP STS 30
COR 29
INT. TEST 28
FRAME 27
TO CTI & 16:9 MOULE
TR 109
TR206
TR 208
4.43 MHz
3.58MHz
TR 205
TO PIN 35 IC 204
IIC BUS
IRR100
IIC BUS
EEPROM IC 101
SOUND STDANDARD SWITCH
TO PIN 10 IC 102
TR 105
3,3 V
TR 108
D 105
QZ100 12 MHz
3,3 V
TR8
5 V
R39
R40
TR7
D5 2,5V
5 V
D 108
D 102
FLYBACK FROM EHT
VERTICAL BLANKING FROM PIN 8 IC 5
TO PIN 23, 24, 25 IC 204
TR 101
TR 102
TR 103
5V
R167
F19PAPER.DRW
E.G. 22 / 04 /2000
FOR VOLTAGE SISTETIZER ONLY
PAINTER

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VIDEO SIGNAL PROCESSING

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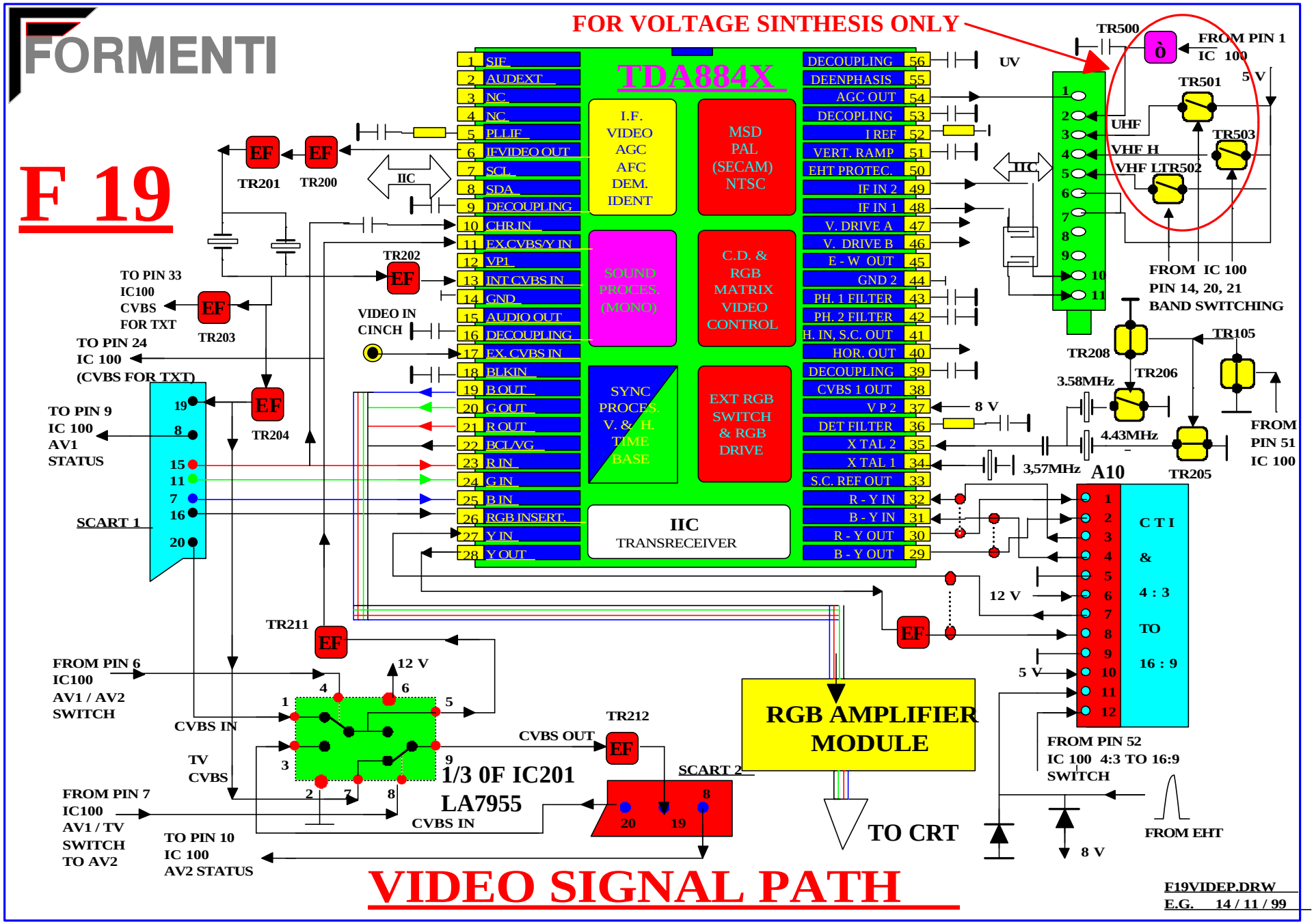
F 19



Reset signal

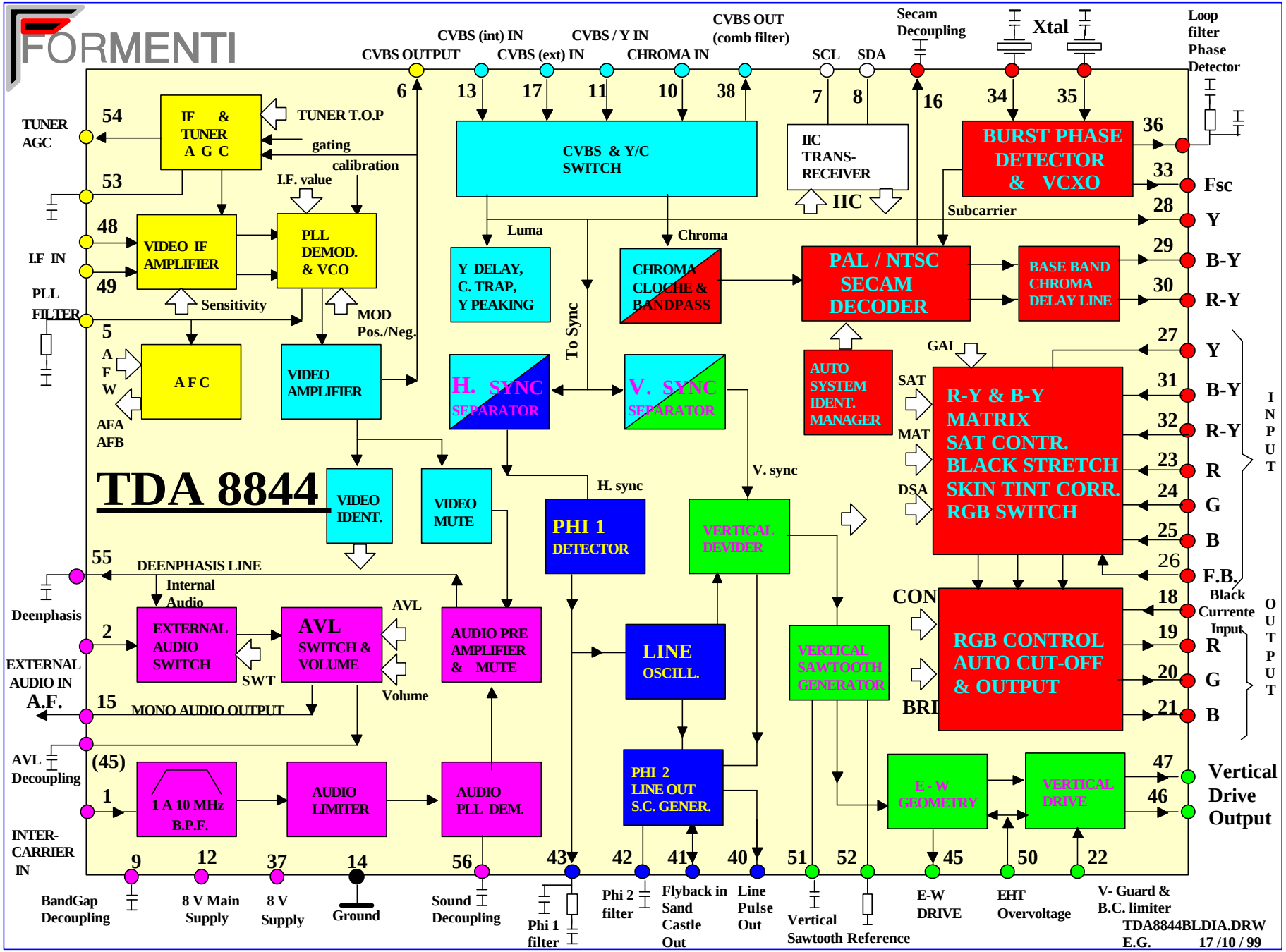
The externally applied RESET signal (active HIGH) is used to initialize the microcontroller core, in addition to the teletext decoder. However, the teletext decoder incorporates a separate internal reset function which is activated on the rising edge of the analog supply pin, V_{DDA}. The purpose of this internal reset circuit is to initialize the teletext decoder when returning from the “text standby mode”.

TDA884X FAMILY SPECIFICATION

FEATURES

The following features are available in all IC’s:

- Multi-standard vision IF circuit with an alignment-freePLL demodulator without external components
- Alignment-free multi-standard FM sound demodulator(4.5 MHz to 6.5 MHz)
- Audio switch
- Flexible source selection with CVBS switch andY(CVBS)/C input so that a comb filter can be applied
- Integrated chrominance trap circuit
- Integrated luminance delay line
- Asymmetrical peaking in the luminance channel with a(defeatable) noise coring function
- Black stretching of non-standard CVBS or luminancesignals
- Integrated chroma band-pass filter with switchablecentre frequency
- Dynamic skin tone control circuit
- Blue stretch circuit which offsets colours near whitetowards blue
- RGB control circuit with “Continuous CathodeCalibration” and white point adjustment
- Possibility to insert a “blue back” option when no videosignal is available
- Horizontal synchronization with two control loops andalignment-free horizontal oscillatoroptimised N2 application.Functionally the IC series is split up is 3 categories, viz:


FORMENTI
TDA 8844
CVBS OUTPUT
CVBS (int) IN
CVBS (ext) IN
CVBS / Y IN
CHROMA IN
CVBS OUT (comb filter)
SCL
SDA
Secam Decoupling
Xtal
Loop filter Phase Detector
TUNER AGC
IF & TUNER A G C
TUNER T.O.P
gating
calibration
I.F. value
I.F IN
PLL FILTER
VIDEO IF AMPLIFIER
PLL DEMOD. & VCO
Sensitivity
MOD Pos./Neg.
A F C
AFA
AFB
VIDEO AMPLIFIER
CVBS & Y/C SWITCH
IIC TRANS-RECEIVER
IIC
BURST PHASE DETECTOR & VCXO
Fsc
Subcarrier
Luma
Chroma
Y DELAY, C. TRAP, Y PEAKING
CHROMA CLOCHE & BANDPASS
PAL / NTSC SECAM DECODER
BASE BAND CHROMA DELAY LINE
Y
B-Y
R-Y
To Sync
H. SYNC SEPARATOR
V. SYNC SEPARATOR
AUTO SYSTEM IDENT. MANAGER
GAI
SAT
MAT
DSA
R-Y & B-Y MATRIX
SAT CONTR.
BLACK STRETCH
SKIN TINT CORR.
RGB SWITCH
R
G
B
F.B.
INPUT
VIDEO IDENT.
VIDEO MUTE
H. sync
V. sync
PHI 1 DETECTOR
VERTICAL DEVIDER
DEENPHASIS LINE
Internal Audio
Deenphasis
EXTERNAL AUDIO SWITCH
AVL SWITCH & VOLUME
SWT
Volume
AVL
AUDIO PRE AMPLIFIER & MUTE
EXTERNAL AUDIO IN
A.F.
MONO AUDIO OUTPUT
LINE OSCILL.
VERTICAL SAWTOOTH GENERATOR
CON
BRI
RGB CONTROL AUTO CUT-OFF & OUTPUT
Black Currente Input
OUTPUT
AVL Decoupling
1 A 10 MHz B.P.F.
AUDIO LIMITER
AUDIO PLL DEM.
PHI 2 LINE OUT S.C. GENER.
E - W GEOMETRY
VERTICAL DRIVE
Vertical Drive Output
INTER-CARRIER IN
BandGap Decoupling
8 V Main Supply
8 V Supply
Ground
Sound Decoupling
Phi 1 filter
Phi 2 filter
Flyback in Sand Castle Out
Line Pulse Out
Vertical Sawtooth Reference
E-W DRIVE
EHT Overvoltage
V- Guard & B.C. limiter
TDA8844BLDIA.DRW
E.G. 17 /10 / 99

- Versions intended to be used in economy TV receiverswith all basic functions (envelope: S-DIP 56 and QFP 64)
- Versions with additional features like E-W geometrycontrol, H-V zoom function and YUV interface which are intended for TV receivers with 110° picture tubes(envelope: S-DIP 56)
- Versions which have in addition a second RGB inputwith saturation control and a second CVBS output (envelope: QFP 64)
- Vertical count-down circuit
- Vertical driver optimised for DC-coupled vertical outputstages

GENERAL DESCRIPTION

The various versions of the TDA 884X/5X series areI 2 C-bus controlled single chip TV processors which are

intended to be applied in PAL, NTSC, PAL/NTSC and multi-standard television receivers. The N2 version is pin and application compatible with the N1 version, however,a new feature has been added which makes the N2 more attractive. The IF PLL demodulator has been replaced byan alignment-free IF PLL demodulator with internal VCO (no tuned circuit required). The setting of the variousfrequencies (33.4, 33.9, 38, 38.9, 45,75 and 58.75 MHz) can be made via the I 2 C-bus.

Because of this difference the N2 version is compatiblewith the N1, however, N1 devices cannot be used in an optimized N2 application

Functionally the IC series is split up is 3 categories, viz:

- Versions intended to be used in economy TV receivers with all basic functions (envelope: S-DIP 56 and QFP 64)
- Versions with additional features like E-W geometry control, H-V zoom function and YUV interface which areintended for TV receivers with 110° picture tubes (envelope: S-DIP 56)
- Versions which have in addition a second RGB input with saturation control and a second CVBS output (envelope: QFP 64)

FUNCTIONAL DESCRIPTION

Vision IF amplifier

The IF-amplifier contains 3 ac-coupled control stages with a total gain control range which is higher then 66 dB. The sensitivity of the circuit is comparable with that of modern

IF-IC's.

The video signal is demodulated by means of an alignment-free PLL carrier regenerator with an internalVCO. This VCO is calibrated by means of a digital control circuit which uses the X-tal frequency of the colour decoder as a reference. The frequency setting for the various standards (33.4, 33.9, 38, 38.9, 45.75 and 58.75 MHz) is realised via the I 2 C-bus. To get a good performance for phase modulated carrier signals the control speed of the PLL can be increased by means of the FFI bit.

The AFC output is generated by the digital control circuit of the IF-PLL demodulator and can be read via the I 2 C-bus.

For fast search tuning systems the window of the AFC can be increased with a factor 3. The setting is realised with the AFW bit. The AFC data is valid only when the horizontal PLL is in lock (SL = 1)

Depending on the type the AGC-detector operates on top-sync level (single standard versions) or on top sync and top white- level (multi standard versions). The demodulation polarity is switched via the I 2 C-bus. The AGC detector time-constant capacitor is connected externally. This mainly because of the flexibility of the application. The time-constant of the AGC system during positive modulation is rather long to avoid visible variations of the signal amplitude. To improve the speed of the AGC system a circuit has been included which detects whether the AGC detector is activated every frame period. When during 3 field periods no action detected the speed of the system is increased. For signals without peak white information the system switches automatically to a gated black level AGC. Because a black level clamp pulse is required for this way of operation the circuit will only switch to black level AGC in the internal mode.

The circuits contain a video identification circuit which is independent of the synchronisation circuit. Therefore search tuning is possible when the display section of the receiver is used as a monitor. However, this ident circuit cannot be made as sensitive as the slower sync ident circuit (SL) and we recommend to use both ident outputs to obtain a reliable search system. The ident output is supplied to the tuning system via the I 2 C-bus.

The input of the identification circuit is connected to pin 13 (S-DIP 56 devices), the "internal" CVBS input (see Fig.6).

This has the advantage that the ident circuit can also be made operative when a scrambled signal is received (descrambler connected between pin 6 (IF video output) and pin 13). A second advantage is that the ident circuit can be used when the IF amplifier is not used (e.g. with built-in satellite tuners).

The video ident circuit can also be used to identify the selected CBVS or Y/C signal. The switching between the 2 modes can be realised with the VIM bit.

Video switches

The circuits have two CVBS inputs (internal and external CVBS) and a Y/C input. When the Y/C input is not required the Y input can be used as third CVBS input. The switch configuration is given in Fig.6. The selection of the various sources is made via the I 2 C-bus.

For the TDA 884X devices the video switch configuration is identical to the switch of the TDA 8374/75 series. So the circuit has one CVBS output (amplitude of 2 VP-P for the TDA884X series) and the I 2 C-bus control is similar to that of the TDA 8374/75. For the TDA 885X IC's the video switch circuit has a second output (amplitude of 1 VP-P) which can be set independently of the position of the first output. The input signal for the decoder is also available on the CVBS1-output.

Therefore this signal can be used to drive the Teletext decoder. If S-VHS is selected for one of the outputs the luminance and chrominance signals are added so that a CVBS signal is obtained again.

Sound circuit

The sound bandpass and trap filters have to be connected externally. The filtered intercarrier signal is fed to a limiter circuit and is demodulated by means of a PLL demodulator. This PLL circuit tunes itself automatically to the incoming carrier signal so that no adjustment is required.

The volume is controlled via the I 2 C-bus. The deemphasis capacitor has to be connected externally. The non-controlled audio signal can be obtained from this pin (via a buffer stage).

The FM demodulator can be muted via the I 2 C-bus. This function can be used to switch-off the sound during a channel change so that high output peaks are prevented.

The TDA 8840/41/42/46 contain an Automatic Volume Levelling (AVL) circuit which automatically stabilises the audio output signal to a certain level which can be set by the viewer by means of the volume control. This function prevents big audio output fluctuations due to variations of the modulation depth of the transmitter. The AVL function can be activated via the I 2 C-bus.

Synchronisation circuit

The sync separator is preceded by a controlled amplifier which adjusts the sync pulse amplitude to a fixed level. These pulses are fed to the slicing stage which is operating at 50% of the amplitude. The separated sync pulses are fed to the first phase detector and to the coincidence detector. This coincidence detector is used to detect whether the line oscillator is synchronised and can also be used for transmitter identification. This circuit can be made less sensitive by means of the STM bit. This mode can be used during search tuning to avoid that the tuning system will stop at very weak input signals. The first PLL has a very high statical steepness so that the phase of the picture is independent of the line frequency.

The horizontal output signal is generated by means of an oscillator which is running at twice the line frequency. Its frequency is divided by 2 to lock the first control loop to the incoming signal. The time-constant of the loop can be forced by the I 2 C-bus (fast or slow). If required the IC can select the time-constant depending on the noise content of the incoming video signal.

The free-running frequency of the oscillator is determined by a digital control circuit which is locked to the reference signal of the colour decoder. When the IC is switched-on the horizontal output signal is suppressed and the oscillator is calibrated as soon as all sub-address bytes have been sent. When the frequency of the oscillator is correct the horizontal drive signal is switched-on. To obtain a smooth switching-on and switching-off behaviour of the horizontal output stage the horizontal output frequency is doubled during switch-on and switch-off (slow start/stop). During that time the duty cycle of the output pulse has such a value that maximum safety is obtained for the output stage.

To protect the horizontal output transistor the horizontal drive is immediately switched off when a power-on-reset is detected. The drive signal is switched-on again when the normal switch-on procedure is followed, i.e. all sub-address bytes must be sent and after calibration the horizontal drive signal will be released again via the slow start procedure. When the coincidence detector indicates an out-of-lock situation the calibration procedure is repeated.

The circuit has a second control loop to generate the drive pulses for the horizontal driver stage. The horizontal output is gated with the flyback pulse so that the horizontal output transistor cannot be switched-on during the flyback time.

Via the I 2 C-bus adjustments can be made of the horizontal and vertical geometry. The vertical sawtooth generator drives the vertical output drive circuit which has a differential output current. For the E-W drive a single ended current output is available. A special

feature is the zoom function for both the horizontal and vertical deflection and the vertical scroll function which are available in some versions. When the horizontal scan is reduced to display 4:3 pictures on a 16:9 picture tube an accurate video blanking can be switched on to obtain well defined edges on the screen.

Overvoltage conditions (X-ray protection) can be detected via the EHT tracking pin. When an overvoltage condition is detected the horizontal output drive signal will be switched-off via the slow stop procedure but it is also possible that the drive is not switched-off and that just a protection indication is given in the I 2 C-bus output byte.

The choice is made via the input bit PRD. The IC's have a second protection input on the φ2 filter capacitor pin. When this input is activated the drive signal is switched-off immediately and switched-on again via the slow start procedure. For this reason this protection input can be used as "flash protection".

The drive pulses for the vertical sawtooth generator are obtained from a vertical countdown circuit. This countdown circuit has various windows depending on the incoming signal (50 Hz or 60 Hz and standard or non standard). The countdown circuit can be forced in various modes by means of the I 2 C-bus. During the insertion of RGB signals the maximum vertical frequency is increased to 72 Hz so that the circuit can also synchronise on signals with a higher vertical frequency like VGA. To obtain short switching times of the countdown circuit during a channel change the divider can be forced in the search window by means of the NCIN bit. The vertical deflection can be set in the de-interlace mode via the I 2 C bus. To avoid damage of the picture tube when the vertical deflection fails the guard output current of the TDA 8350/51 can be supplied to the beam current limiting input. When a failure is detected the RGB-outputs are blanked and a bit is set (NDF) in the status byte of the I 2 C-bus. When no vertical deflection output stage is connected thisguard circuit will also blank the output signals. This can be overruled by means of the EVG bit.

Chroma and luminance processing

The circuits contain a chroma bandpass and trap circuit. The filters are realised by means of gyrator circuits and

they are automatically calibrated by comparing the tuning frequency with the X-tal frequency of the decoder. The luminance delay line and the delay for the peaking circuit are also realised by means of gyrator circuits. The centre frequency of the chroma bandpass filter is switchable via the I 2 C-bus so that the performance can be optimised for

“front-end” signals and external CVBS signals. During SECAM reception the centre frequency of the chroma trap is reduced to get a better suppression of the SECAM carrier frequencies. All IC’s have a black stretcher circuit which corrects the black level for incoming video signals which have a deviation between the black level and the blanking level (back porch). The timeconstant for the black stretcher is realised internally.
The resolution of the peaking control DAC has been increased to 6 bits. All IC’s have a defeatable coringfunction in the peaking circuit. Some of these IC’s have a YUV interface (see table on page 2) so that picture improvement IC’s like the TDA 9170 (Contrast improvement), TDA 9177 (Sharpness improvement) and TDA 4556/66 (CTI) can be applied. When the CTI IC’s are applied it is possible to increase the gain of the luminance channel by means of the GAI bit in subaddress 03 so that the resulting RGB output signals are not affected.

Colour decoder

Depending on the IC type the colour decoder can decode PAL, PAL/NTSC or PAL/NTSC/SECAM signals. The PAL/NTSC decoder contains an alignment-free X-tal oscillator, a killer circuit and two colour difference demodulators. The 90° phase shift for the reference signal is made internally.
The IC’s contain an Automatic Colour Limiting (ACL) circuit which is switchable via the I 2 C-bus and which prevents that oversaturation occurs when signals with a high chroma-to-burst ratio are received. The ACL circuit is designed such that it only reduces the chroma signal and not the burst signal. This has the advantage that the colour sensitivity is not affected by this function. The SECAM decoder contains an auto-calibrating PLL demodulator which has two references, viz: the 4.4 MHz sub-carrier frequency which is obtained from the X-tal oscillator which is used to tune the PLL to the desired free-running frequency and the bandgap reference to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical blanking period, when the IC is in search or SECAM mode.
The frequency of the active X-tal is fed to the Fsc output (pin 33) and can be used to tune an external comb filter (e.g. the SAA 4961).
The base-band delay line (TDA 4665 function) is integrated in the PAL/SECAM IC’s and in the NTSC IC TDA 8846A. In the latter IC it improves the cross colour performance (chroma comb filter). The demodulated colour difference signals are internally supplied to the delay line. The colour difference matrix switches automatically between PAL/SECAM and NTSC, however, it is also possible to fix the matrix in the PAL standard.

The “blue stretch” circuit is intended to shift colour near “white” with sufficient contrast values towards more blue to obtain a brighter impression of the picture.
Which colour standard the IC’s can decode depends on the external X-tals. The X-tal to be connected to pin 34 must have a frequency of 3.5 MHz (NTSC-M, PAL-M or PAL-N) and pin 35 can handle X-tals with a frequency of 4.4 and 3.5 MHz. Because the X-tal frequency is used to tune the line oscillator the value of the X-tal frequency must be given to the IC via the I 2 C-bus. It is also possible to use the IC in the so called “Tri-norma” mode for South America. In that case one X-tal must be connected to pin 34 and the other 2 to pin 35. The switching between the 2 latter X-tals must be done externally. This has the consequence that the search loop of the decoder must be controlled by the µ-computer. To prevent calibration problems of the horizontal oscillator the external switching between the 2 X-tals should be carried out when the oscillator is forced to pin 34. For a reliable calibration of the horizontal oscillator it is very important that the X-tal indication bits (XA and XB) are not corrupted. For this reason the X-tal bits can be read in the output bytes so that the software can check the I 2 C-bus transmission.
Under bad-signal conditions (e.g. VCR-playback in feature mode), it may occur that the colour killer is activated although the colour PLL is still in lock. When this killing action is not wanted it is possible to overrule the colour killer by forcing the colour decoder to the required standard and to activate the FCO-bit (Forced Colour On) in the control-5 subaddress.
The IC’s contain a so-called “Dynamic skin tone (flesh) control” feature. This function is realised in the YUV domain by detecting the colours near to the skin tone. The correction angle can be controlled via the I 2 C-bus.

RGB output circuit and black-current stabilisation

The colour-difference signals are matrixed with the luminance signal to obtain the RGB-signals. The TDA 884X devices have one (linear) RGB input. This RGB signal can be controlled on contrast and brightness (like TDA 8374/75). By means of the IE1 bit the insertion blanking can be switched on or off. Via the IN1 bit it can be read whether the insertion pin has a high level or not.
The TDA 885X IC’s have an additional RGB input. This RGB signal can be controlled on contrast, saturation and brightness. The insertion blanking of this input can be switched-off by means of the IE2 bit. Via the IN2 bit it can be read whether the insertion pin has a high level or not.

The output signal has an amplitude of about 2 volts black-to-white at nominal input signals and nominal settings of the controls. To increase the flexibility of the IC it is possible to insert OSD and/or teletext signals directly at the RGB outputs. This insertion mode is controlled via the insertion input (pin 26 in the S-DIP 56- and pin 38 in the QFP-64 envelope). This blanking action at the RGB outputs has some delay which must be compensated externally.

To obtain an accurate biasing of the picture tube a “Continuous Cathode Calibration” circuit has been developed. This function is realised by means of a 2-point black level stabilisation circuit. By inserting 2 test levels for each gun and comparing the resulting cathode currents with 2 different reference currents the influence of the picture tube parameters like the spread in cut-off voltage can be eliminated.

This 2-point stabilisation is based on the principle that the ratio between the cathode currents is coupled to the ratio between the drive voltages according to:

$$[\, I_{ki} \,/\, I_{k2} \,] = [\, V_{dr1} \,/\, V_{dr2} \,]$$

The feedback loop makes the ratio between the cathode currents Ik1 and Ik2 equal to the ratio between the reference currents (which are internally fixed) by changing the (black) level and the amplitude of the RGB output signals via 2 converging loops. The system operates in such a way that the black level of the drive signal is controlled to the cut-off point of the gun so that a very good grey scale tracking is obtained. The accuracy of the adjustment of the black level is just dependent on the ratio of internal currents and these can be made very accurately in integrated circuits. An additional advantage of the 2-point measurement is that the control system makes the absolute value of Ik1 and Ik2 identical to the internal reference currents. Because this adjustment is obtained by means of an adaption of the gain of the RGB control stage this control stabilises the gain of the complete channel (RGB output stage and cathode characteristic).

As a result variations in the gain figures during life will be compensated by this 2-point loop.

An important property of the 2-point stabilisation is that the off-set as well as the gain of the RGB path is adjusted by the feedback loop. Hence the maximum drive voltage for the cathode is fixed by the relation between the test pulses, the reference current and the relative gain setting of the 3 channels. This has the consequence that the drive level of the CRT cannot be adjusted by adapting the gain of the RGB output stage. Because different picture tubes may require different drive levels the typical “cathode drive level” amplitude can be adjusted by means of an I 2 C-bus setting. Dependent on the chosen cathode drive

level the typical gain of the RGB output stages can be fixed taking into account the drive capability of the RGB outputs (pins 19 to 21). More details about the design will be given in the application report.

The measurement of the “high” and the “low” current of the 2- point stabilisation circuit is carried out in 2 consecutive fields. The leakage current is measured in each field. The maximum allowable leakage current is 100 μA When the TV receiver is switched-on the RGB output signals are blanked and the black current loop will try to set the right picture tube bias levels. Via the AST bit a choice can be made between automatic start-up or a start-up via the μ-processor. In the automatic mode the RGB drive signals are switched-on as soon as the black current loop

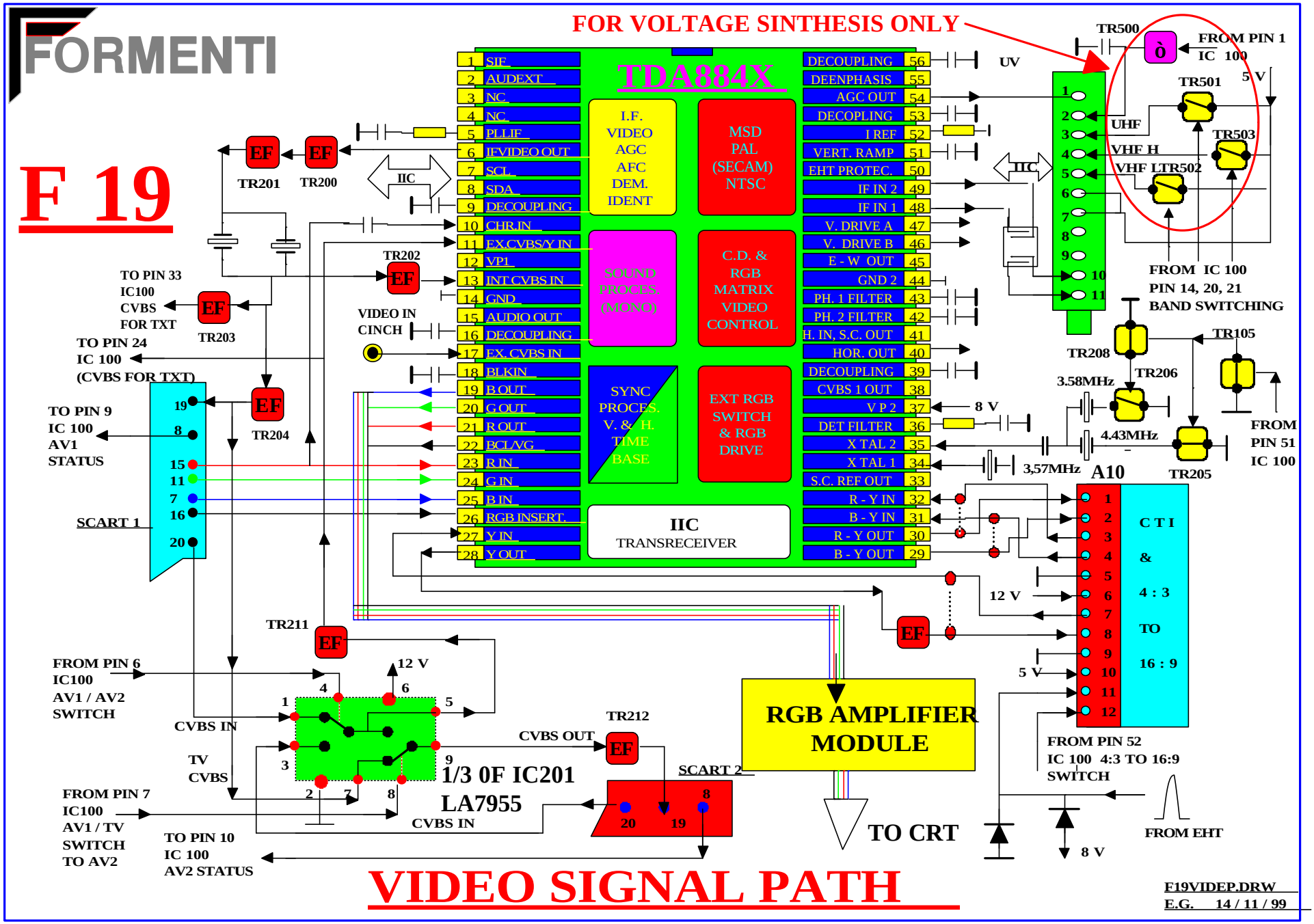
has been stabilised. In the other mode the BCF bit is set to 0 when the loop is stabilised. The RGB drive can than be switched-on by setting the AST bit to 0. In the latter mod some delay can be introduced between the setting of the BCF bit and the switching of the AST bit so that switch-on effects can be suppressed. It is also possible to start-up the devices with a fixed internal delay (as with the TDA 837X and the TDA884X/5X N1). This mode is activated with the BCO bit.

The vertical blanking is adapted to the incoming CVBS signal (50 Hz or 60 Hz). When the flyback time of the vertical output stage is longer than the 60 Hz blanking time the blanking can be increased to the same value as that of the 50 Hz blanking. This can be set by means of the LBM bit.

For an easy (manual) adjustment of the Vg2 control voltage the VSD bit is available. When this bit is activated the black current loop is switched-off, a fixed black level is inserted at the RGB outputs and the vertical scan is switched-off so that a horizontal line is displayed on the screen. This line can be used as indicator for the Vg2 adjustment. Because of the different requirements for the optimum cut-off voltage of the picture tube the RGB output level is adjustable when the VSD bit is activated. The control range is 2.5 ± 0.7 V and can be controlled via the brightness control DAC. It is possible to insert a so called “blue back” back-ground level when no video is available. This feature can be activated via the BB bit in the control2 subaddress.

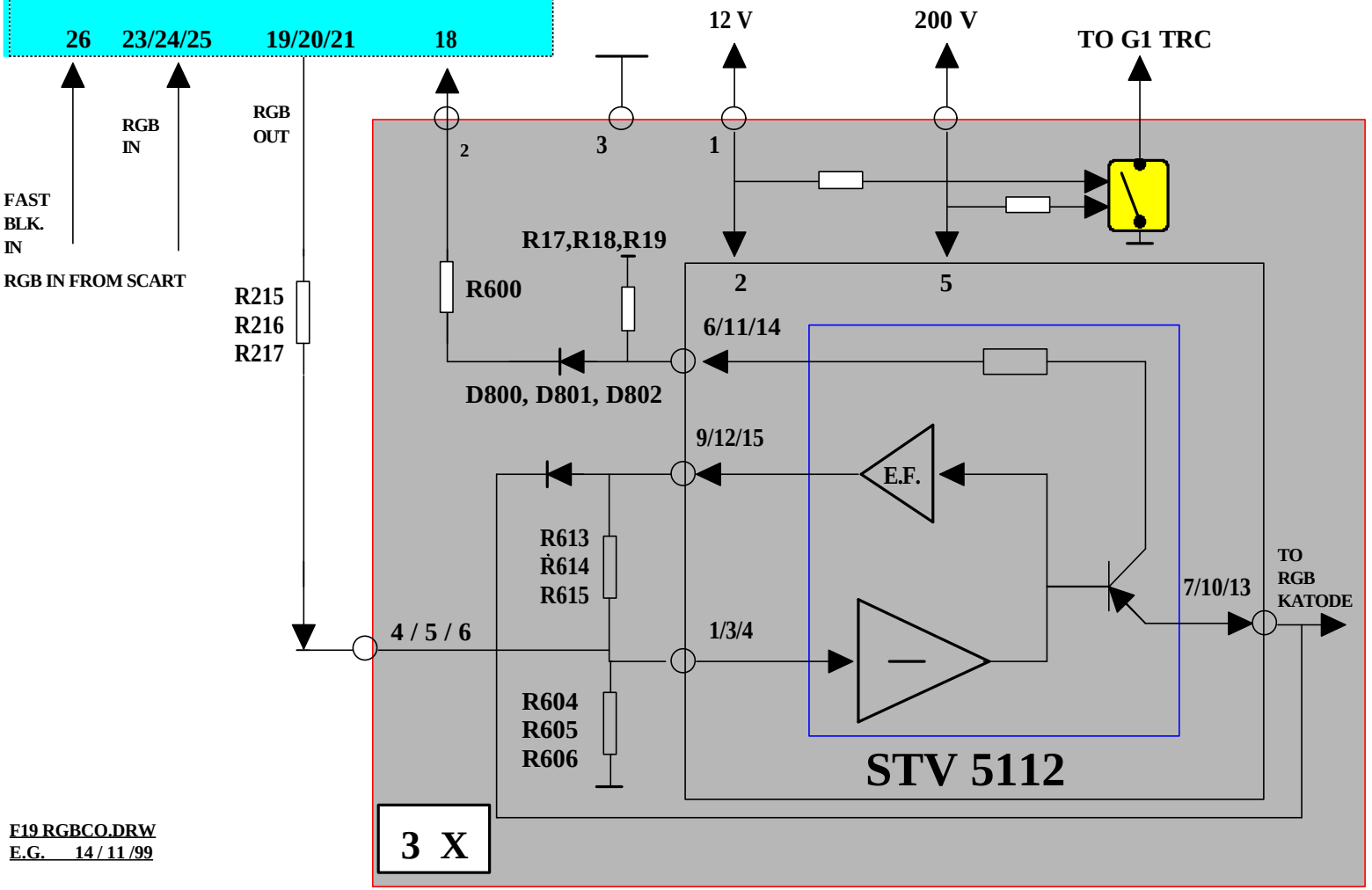
FORMENTI

F 19



FORMENTI

F19 RGB AMPLIFIER



F19 RGBCO.DRW
E.G. 14 / 11 /99

FORMENTI

F 19 FEATURE MODULE

Colour Transient Improvment

&

4 : 3 to 16 : 9 Signal Processing

SAA4981

Monolithic integrated 16 : 9 Compressor

FEATURES

- Fixed horizontal compression by a factor of 4 ¤3 for most video standards
- Three fixed screen positions (left, centre and right)
- 5 MHz bandwidth
- Bypass function
- Inputs for luminance and chrominance of side panels
- Standard video inputs and outputs (Y, (B-Y) and (P-Y))
- Horizontal and vertical sync signals are not processed
- Pre filters and post filters on chip.

GENERAL DESCRIPTION

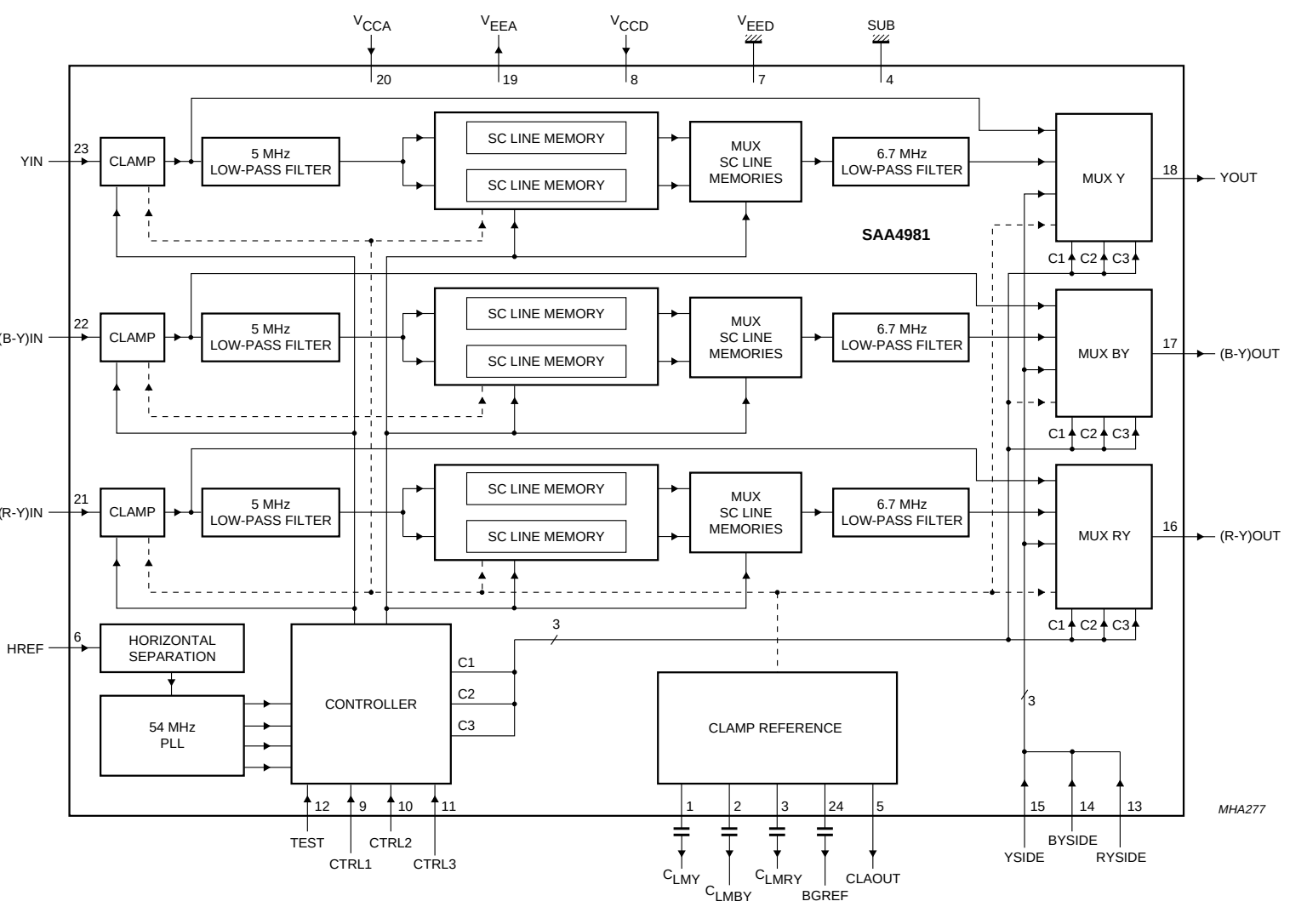
The integrated 16 : 9 compressor is an IC which compresses the active part of a video line by a factor of 4 ¤3 from, for example, 52 ms to 39ms. This is necessary to display 4:3 video software on a 16 : 9 tube in the correctproportion. The capacitively coupled video inputs are Y, (B-Y) and (P-Y).

The synchronisation input HREF is a line frequencyreference signal. The bandwidth of the IC is up to 5 MHz and the signal delay is realized with SC Line Memories (Switched Capacitors Line Memories). The output of the 16 : 9 compressor also has the format Y, (B Y) and (P-Y) and provides the following two possibilities:

1. Bypass function (the input signal is not compressed)
2. Compressed video by a factor of 4 ¤3 with three different fixed screen positions (left, centre and right). The luminance and chrominance of the side panels are determined by the external signals YSIDE, BYSIDE and RYSIDE.

The horizontal compression is a time discrete and amplitude continuous signal processing. This provides pre and post filters which are realized on-chip.

FUNCTIONAL DESCRIPTION


V_{CCA}
V_{EEA}
V_{CCD}
V_{EED}
SUB
20
19
8
7
4
YIN
23
CLAMP
5 MHz LOW-PASS FILTER
SC LINE MEMORY
SC LINE MEMORY
MUX SC LINE MEMORIES
6.7 MHz LOW-PASS FILTER
MUX Y
18
YOUT
SAA4981
C1
C2
C3
(B-Y)IN
22
CLAMP
5 MHz LOW-PASS FILTER
SC LINE MEMORY
SC LINE MEMORY
MUX SC LINE MEMORIES
6.7 MHz LOW-PASS FILTER
MUX BY
17
(B-Y)OUT
C1
C2
C3
(R-Y)IN
21
CLAMP
5 MHz LOW-PASS FILTER
SC LINE MEMORY
SC LINE MEMORY
MUX SC LINE MEMORIES
6.7 MHz LOW-PASS FILTER
MUX RY
16
(R-Y)OUT
C1
C2
C3
HREF
6
HORIZONTAL SEPARATION
54 MHz PLL
CONTROLLER
C1
C2
C3
3
CLAMP REFERENCE
3
12
9
10
11
TEST
CTRL1
CTRL2
CTRL3
1
2
3
24
5
C_{LMY}
C_{LMBY}
C_{LMRY}
BGREF
CLAOUT
15
14
13
YSIDE
BYSIDE
RYSIDE
MHA277

Applicable video standards

The integrated 16 : 9 compressor can be used for the following video standards; B, C, D, G, H, I, K, K1, L, M and N. standards D, I, K, K1 and L will show a reducedvideo bandwidth above 5 MHz.

Clamping circuit

The clamping circuits clamp the video input signals Y, (B-Y) and (P-Y) to the DC level of the clamp reference signal fed from the clamp reference circuit. This is necessary to ensure that the input signals are in the correct input voltage range for the 5 MHz low-pass filters and the SC line memories.

Internal pre filters

Before the signals are sampled in the time discrete and amplitude continuous area, low-pass filtering is necessary to avoid any aliasing. Even if the inputs have already been low-pass filtered further filtering is advantageous for the electromagnetic compatibility (EMC). The same transfer function is used for all three low-pass filters because of the same bandwidth for the luminance and chrominance signals (up to 5 MHz)

SC line memories

After the low-pass filters the input signals are fed to the SC line memories. The signals are sampled at a clock frequency of 13.5 MHz. One video line later the signals are read with a clock frequency of 18 MHz in the compression mode. The result of the different clock frequencies is a horizontal compression by a factor of 4 ¤3 . The clocks and the horizontal starting pulses for the SC line memories are fed from the controller.

Two line memories are required for each signal path because in the compression mode, in one video line the signals are sampled to the SC line memories with 13.5 MHz and one video line later the signals are read with 18 MHz. In the bypass mode, via the SC line memories, in one video line the signals are sampled with 13.5 MHz and one video line later the signals are read with 13.5 MHz.

The SC line memories are suitable for signals with a bandwidth up to 5 MHz. With a multiplexer (MUX) behind the SC line memories, the sampled video signal is connected to the internal post filters.

Output multiplexer MUX Y, MUX (B-Y) and MUX (P-Y)

The output multiplexers are controlled via C1 and C2 fed from the controller. The multiplexers are used to connect one of the four input signals to the output and, also, enable fast switching.

The input signals of the multiplexers for one component

- The output signal of the post filter
- The uncompressed signal after the input clamping
- The clamping reference signal
- The signal for the side panel determined by YSIDE, BYSIDE and RYSIDE.

The horizontal separation circuit

The 54 MHz horizontal PLL is locked to the positive edge of the digital HREF signal, which is generated in the positive edge of the burst key of a sandcastle signal.

54 MHz horizontal PLL

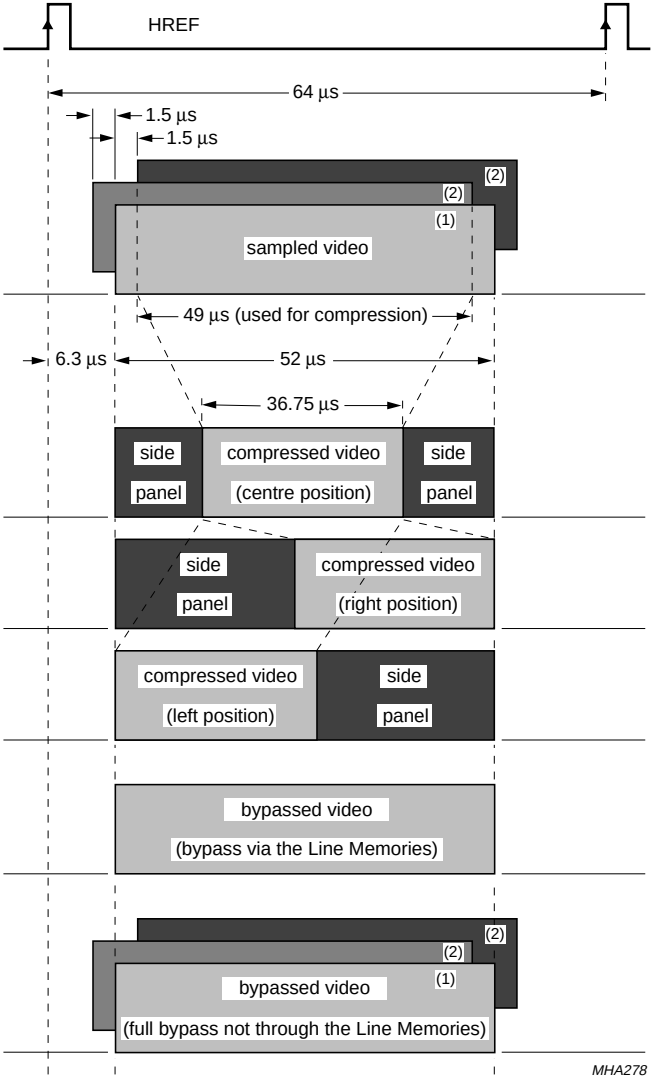
The 13.5 MHz clock frequency for the sampling clock and the 18 MHz clock frequency for the reading clock are generated in the 54 MHz horizontal PLL. The 13.5 MHzclock and the 18 MHz clock are line locked.

Clamp reference

Reference voltages are generated In the clamp reference block. These DC signals are used in the clamping circuits as input signals for the output multiplexers and as reference voltages for the SC line memories. Four external capacitors at the pins CLMY , CLMBY , CLMRY and BGREF respectively are necessary to provide smoothing for the reference voltages. A black level reference signal is available at CLAOUT.

Controller

The controller generates the clocks and the horizontal start signals for the SC line memories and, also, the control signals for the output multiplexers. The timing for the start reading signal for three different screen positions (left, centre and right) and the control signals for the multiplexers (C1 and C2) is fixed. For the uncompressed signals a bypass via the SC line memories and a bypass not via the SC line memories is available. When the signals do not pass the line memories, the frequencyresponse is not affected by the si-function.


HREF
64 µs
1.5 µs
1.5 µs
(2)
(2)
(1)
sampled video
49 µs (used for compression)
6.3 µs
52 µs
36.75 µs
side
panel
compressed video
(centre position)
side
panel
side
panel
compressed video
(right position)
compressed video
(left position)
side
panel
bypassed video
(bypass via the Line Memories)
(2)
(2)
(1)
bypassed video
(full bypass not through the Line Memories)
MHA278

TDA4566

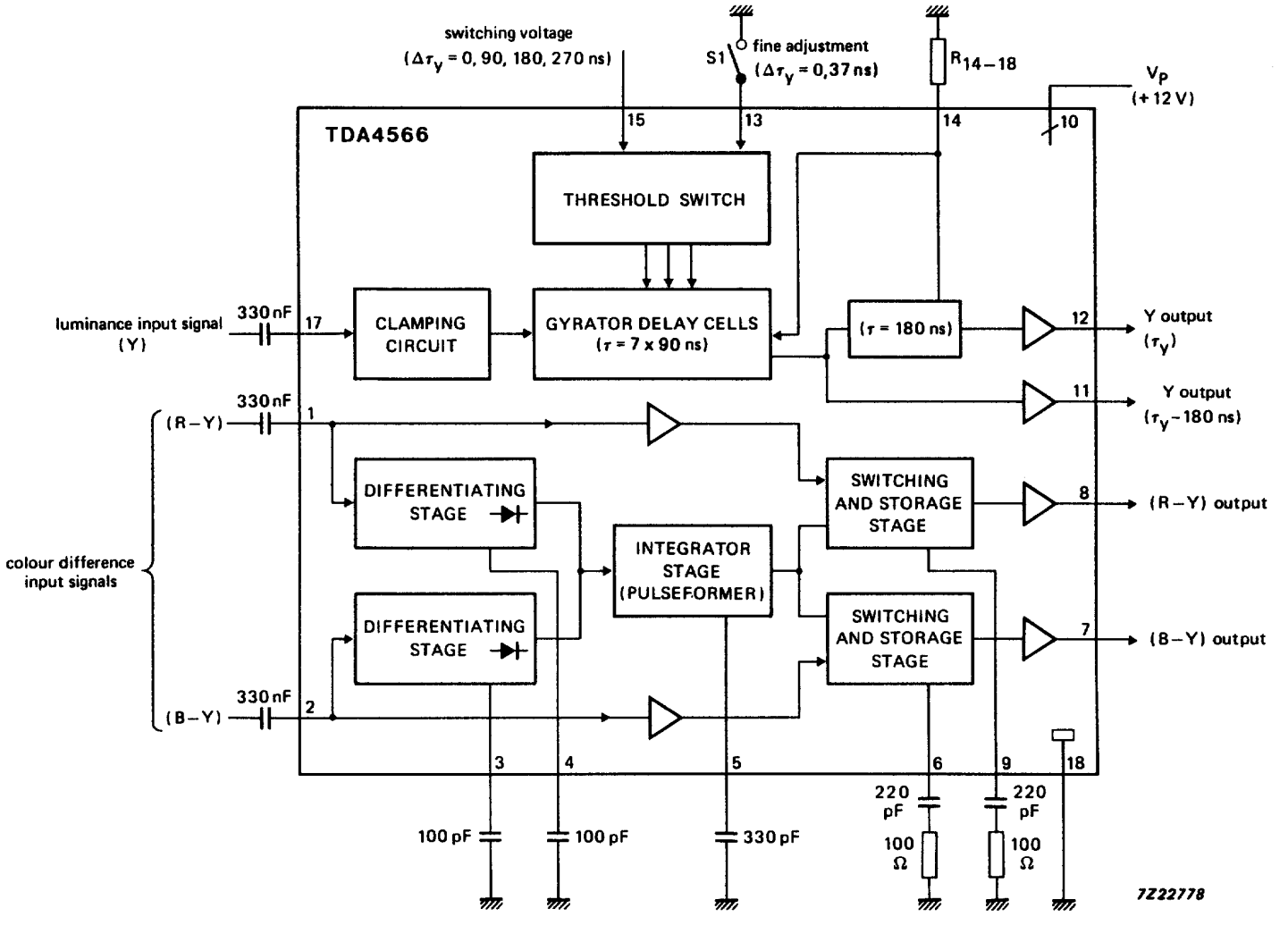
Colour transient improvement circuit

GENERAL DESCRIPTION

The TDA4566 is a monolithic integrated circuit for colour-transient improvement (CTI) and luminance delay line in gyrator technique in colour television receivers.

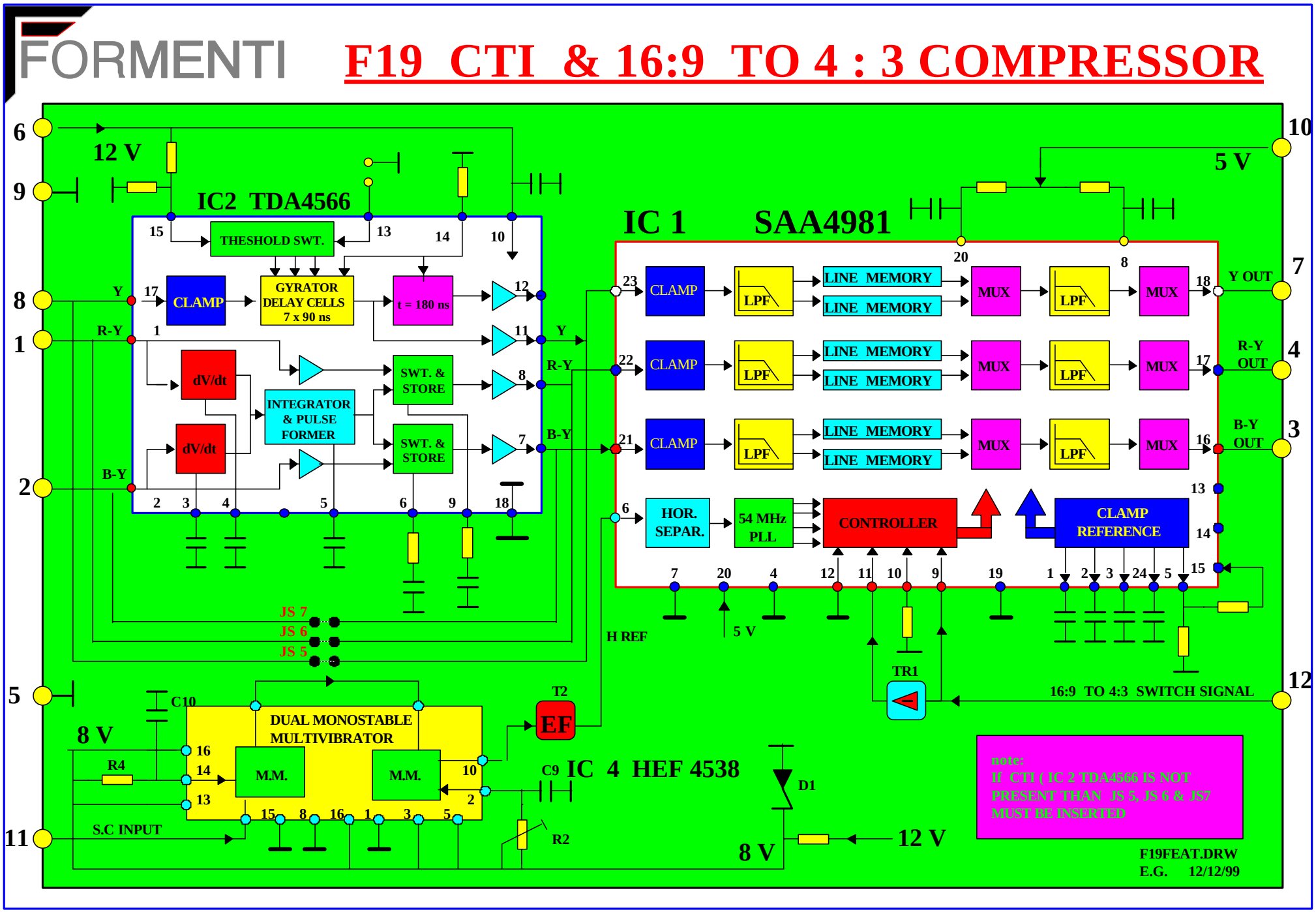
Features

- Colour transient improvement for colour difference signals (R-Y) and (B-Y) with transient detecting-, storage- and switching stages resulting in high transients of colour difference output signals
- A luminance signal path (Y) which substitutes the conventional Y-delay coil with an integrated Y-delay line
- Switchable delay time from 550 ns to 820 ns in steps of 90 ns and additional fine adjustment of 37 ns
- Two Y output signals; one of 180 ns less delay


switching voltage
($\Delta\tau_y$ = 0, 90, 180, 270 ns)
S1
fine adjustment
($\Delta\tau_y$ = 0,37 ns)
R_{14-18}
V_P
(+12 V)
TDA4566
15
13
14
10
THRESHOLD SWITCH
luminance input signal
(Y)
330 nF
17
CLAMPING CIRCUIT
GYRATOR DELAY CELLS
(τ = 7 x 90 ns)
(τ = 180 ns)
12
Y output
(τ_y)
11
Y output
(τ_y - 180 ns)
330 nF
(R-Y)
1
DIFFERENTIATING STAGE
SWITCHING AND STORAGE STAGE
8
(R-Y) output
colour difference input signals
INTEGRATOR STAGE (PULSEFORMER)
DIFFERENTIATING STAGE
SWITCHING AND STORAGE STAGE
7
(B-Y) output
330 nF
(B-Y)
2
3
4
5
6
9
18
100 pF
100 pF
330 pF
220 pF
100 Ω
220 pF
100 Ω
7Z22778

FORMENTI

F19 CTI & 16:9 TO 4 : 3 COMPRESSOR



FORMENTI

SCANNING

SECTION

TDA8351

DC-coupled vertical deflection Circuit

FEATURES

Few external components

Highly efficient fully DC-coupled vertical output bridge circuit

Vertical flyback switch

Guard circuit

Protection against:

- short-circuit of the output pins (7 and 4)
- short-circuit of the output pins to VP
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A guard signal in zoom mode.
-

GENERAL DESCRIPTION

The TDA8351 is a power circuit for use in 9 and 11 colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (RM) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8376 which deliver symmetrical current signals. An external resistor (RCON) connected between the differential input determines the output current through the deflection coil.

The relationship between the differential input current and the output current is defined by: Idiff RCON =Icoil RM .

The output current is adjustable from 0.5 A (p-p) to 3 A(p-p) by varying RM . The maximum input differential voltage is 1.8 V. In the application it is recommended that Vdiff = 1.5 V (typ). This is recommended because of the spread of input current and the spread in the value of RCON .

The flyback voltage is determined by an additional supply voltage VFB . The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage VP optimum for the scan voltage and the second supply voltage VFB optimum for the flyback voltage. Using this method, very high efficiency is achieved.

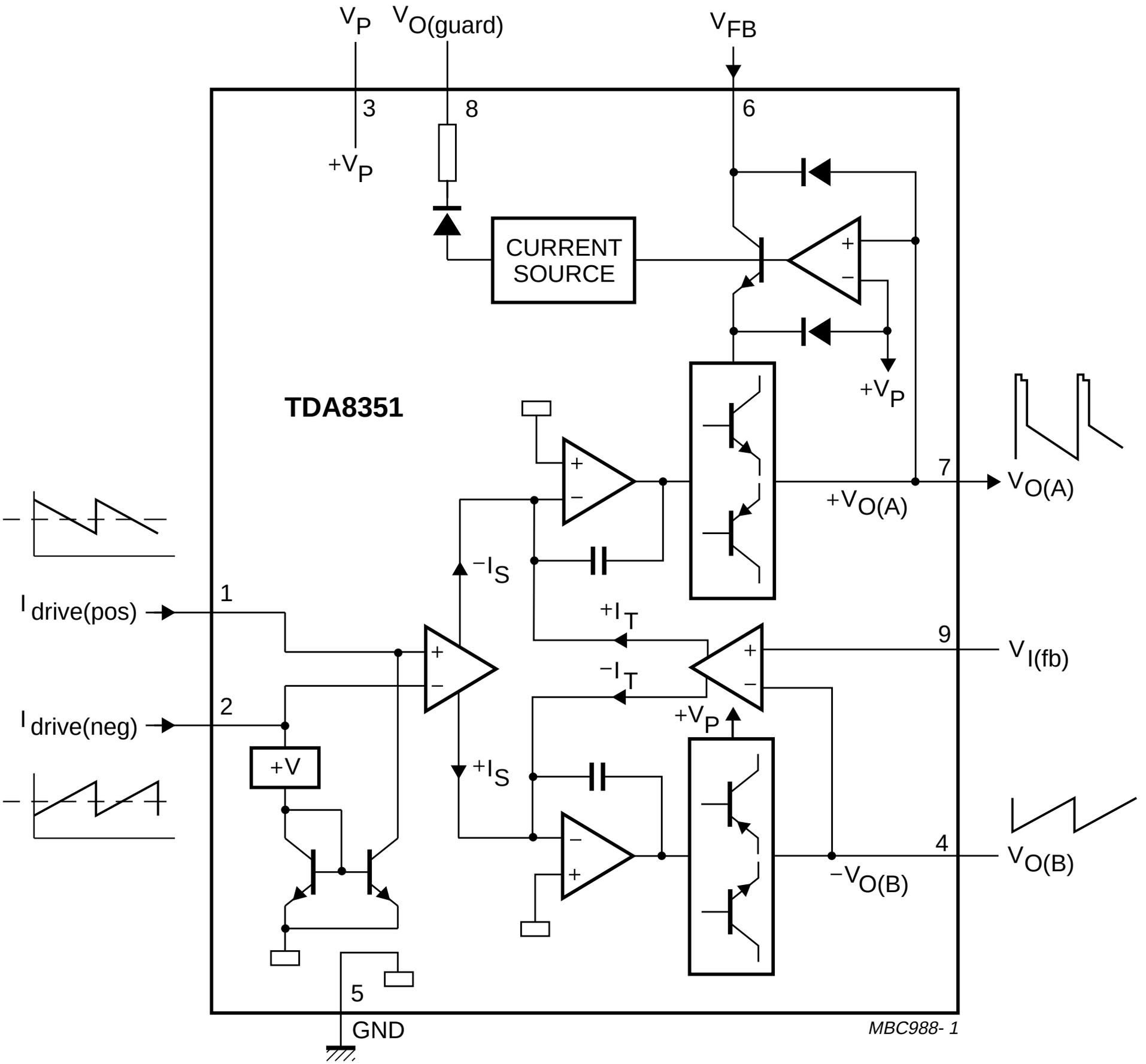
The supply voltage VFB is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

thermal protection

- short-circuit protection of the output pins (pins 4 and 7)
- short-circuit of the output pins to VP .

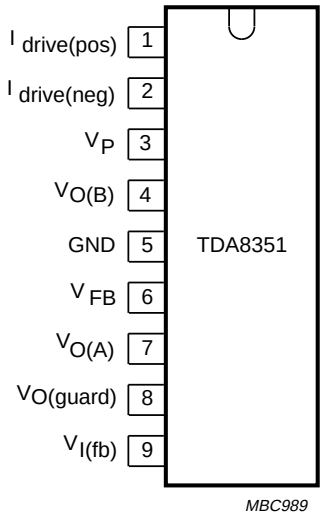
A guard circuit VO(guard) is provided. The guard circuit is activated at the following conditions:

- during flyback
- during short-circuit of the coil and during short-circuit of the output pins (pins 4 and 7) to VP or ground
- during open loop
- when the thermal protection is activated. This signal can be used for blanking the picture tubescreen.


V_P
V_O(guard)
V_FB
3
8
6
+V_P
CURRENT SOURCE
TDA8351
+V_P
7
V_O(A)
+V_O(A)
−I_S
1
I drive(pos)
+I_T
9
V_I(fb)
−I_T
2
I drive(neg)
+V_P
+V
+I_S
4
V_O(B)
−V_O(B)
5
GND
MBC988- 1

PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
V_P	3	operating supply voltage
$V_{O(B)}$	4	output voltage B
GND	5	ground
V_{FB}	6	input flyback supply voltage
$V_{O(A)}$	7	output voltage A
$V_{O(guard)}$	8	guard output voltage
$V_{I(fb)}$	9	input feedback voltage



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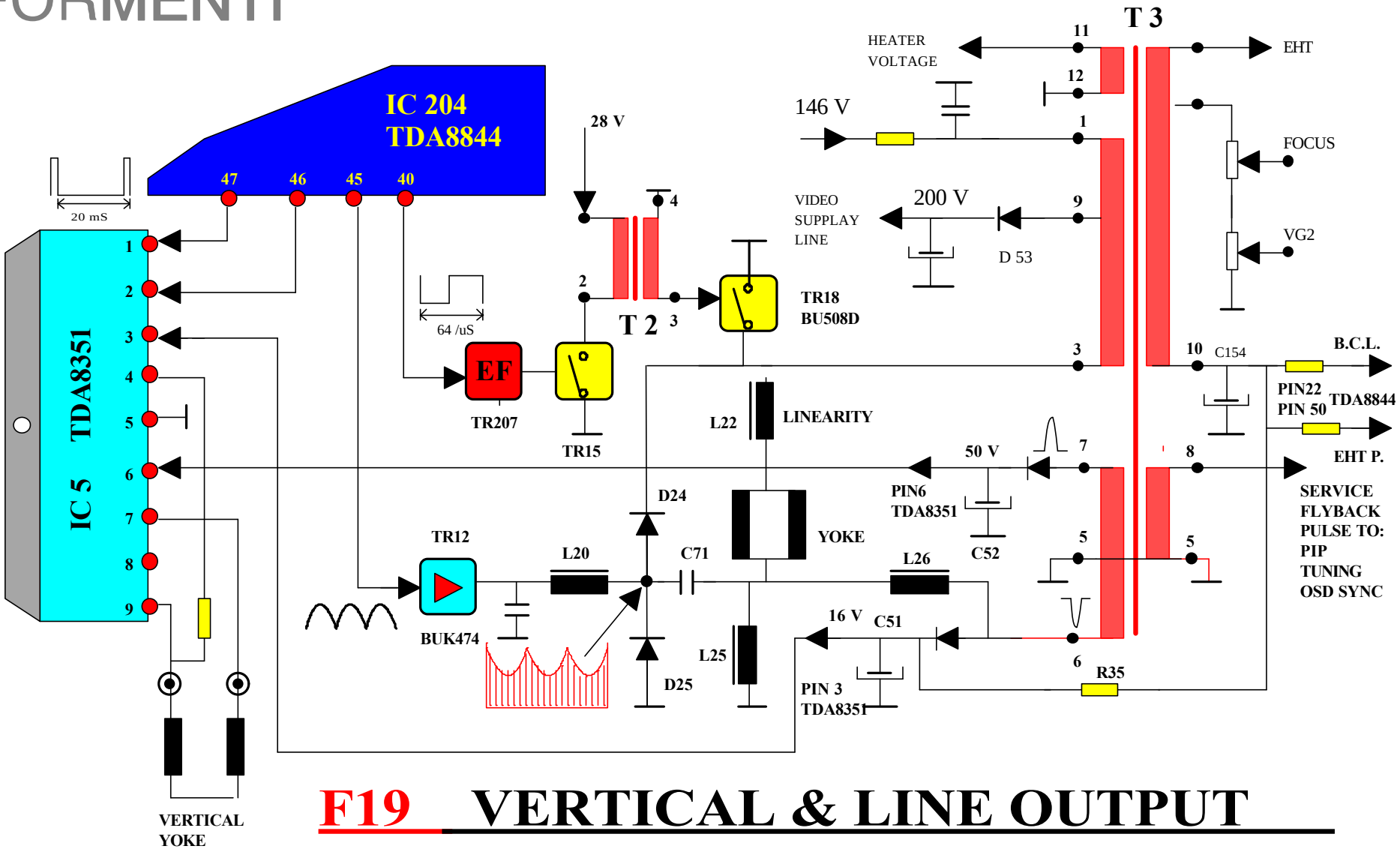
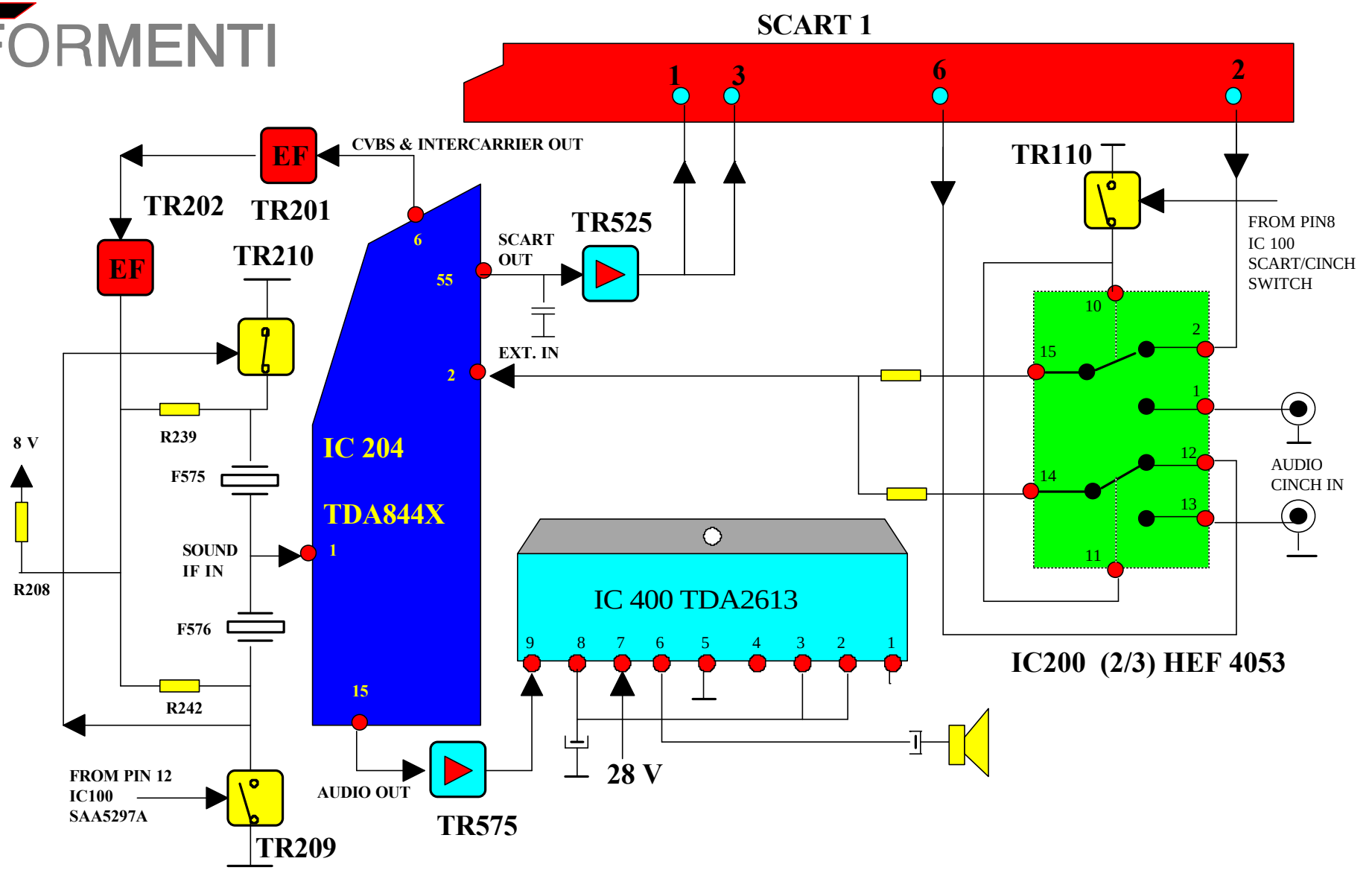


F19 VERTICAL & LINE OUTPUT PLUS E-W CORRECTION

F19 V&HDF.DRW
E.G. 27/12/99

AUDIO SECTION

FORMENTI



F19 AUDIO MONO SIGNAL PATH

F19AMSPH.DRW
E.G. 29/12799

TDA 9870A & TDA9875A MAIN CHARACTERISTICS

FEATURES

Demodulator and decoder section

- Sound IF (SIF) input switch e.g. to select between terrestrial TV SIF and SAT SIF sources SIF AGC with 24 dB control range SIF 8-bit Analog-to-Digital Converter (ADC)
- DQPSK demodulation for different standards, simultaneously with 1-channel FM demodulation NICAM decoding (B/G, I and L standard) Two-carrier multistandard FM demodulation (B/G, D/K and M standard
- Decoding for three analog multi-channel systems (A2, A2+ and A2*) and satellite sound Optional AM demodulation for system L, simultaneously with NICAM
- Programmable identification (B/G, D/K and M standard) and different identification times.
- **DSP section**
- Digital crossbar switch for all digital signal sources and destinations
- Control of volume, balance, contour, bass, treble,
- pseudo stereo, spatial, bass boost and soft-mute
- Plop-free volume control
- Automatic Volume Level (AVL) control
- Adaptive de-emphasis for satellite
- Programmable beeper
- Monitor selection for FM/AM DC values and signals, with peak detection option I 2 S-bus interface for a feature extension (e.g. Dolby surround) with matrix, level adjust and mute.
- **Analog audio section**
- Analog crossbar switch with inputs for mono and stereo

- (also applicable as SCART 3 input), SCART 1
- input/output, SCART 2 input/output and line output
- User defined full-level/ 3 dB scaling for SCART outputs
- Output selection of mono, stereo, dual A/B, dual A or Dual B
- 20 kHz bandwidth for SCART-to-SCART copies
- Standby mode with functionality for SCART copies
- Dual audio digital-to-analog converter from DSP to analog crossbar switch, bandwidth 15 kHz Dual audio ADC from analog inputs to DSP Two dual audio Digital-to-Analog Converters (DACs) for loudspeaker (Main) and headphone (Auxiliary) outputs; also applicable for L, R, C and S in the Dolby Pro Logic mode with feature extension.

GENERAL DESCRIPTION

The TDA9875A is a single-chip Digital TV Sound Processor (DTVSP) for analog and digital multi-channel sound systems in TV sets and satellite receivers.

Supported standards

The multistandard/multi-stereo capability of the TDA9875A is mainly of interest in Europe, but also in Hong Kong/Peoples Republic of China and South East Asia. This includes B/G, D/K, I, M and L standard. In other application areas there exists only subsets of those standard combinations otherwise only single standards are transmitted.

M standard is transmitted in Europe by the American Forces Network (AFN) with European channel spacing (7 MHz VHF, 8 MHz UHF) and monaural sound. The AM sound of L/L' standard is normally demodulated in the 1st sound IF. The resulting AF signal has to be entered into the mono audio input of the TDA9875A. A second possibility is to use the internal AM demodulator stage, however this gives limited performance. Korea has a stereo sound system similar to Europe and is supported by the TDA9875A. Differences include deviation, modulation contents and identification. It is based on M standard.

FUNCTIONAL DESCRIPTION

Description of the demodulator and decoder section

SIF INPUT

Two input pins are provided, SIF1 e.g. for terrestrial TV and SIF2 e.g. for a satellite tuner. For higher SIF signal levels the SIF input can be attenuated with an internal switchable 10 dB resistor divider. As no specific filters are integrated, both inputs have the same specification giving flexibility in application. The selected signal is passed through an AGC circuit and then digitized by an 8-bit ADC operating at 24.576 MHz.

AGC

The gain of the AGC amplifier is controlled from the ADC output by means of a digital control loop employing hysteresis. The AGC has a fast attack behaviour to prevent ADC overloads and a slow decay behaviour to prevent AGC oscillations. For AM demodulation the AGC must be switched off. When switched off, the control loop is reset and fixed gain settings can be chosen from Table 15 (subaddress 0).

MIXER

The digitized input signal is fed to the mixers, which mix one or both input sound carriers down to zero IF. A 24-bit control word for each carrier sets the required frequency. Access to the mixer control word registers is via the I 2 C-bus. When receiving NICAM programs, a feedback signal is added to the control word of the second carrier mixer to establish a carrier-frequency loop.

FM AND AM DEMODULATION

An FM or AM input signal is fed via a band-limiting filter to a demodulator that can be used for either FM or AM demodulation. Apart from the standard (fixed) de-emphasis characteristic, an adaptive de-emphasis is available for encoded satellite programs. A stereo decoder recovers the left and right signal channels from the demodulated sound carriers. Both the European and Korean stereo systems are supported.

FM IDENTIFICATION

The identification of the FM sound mode is performed by AM synchronous demodulation of the pilot signal and narrow-band detection of the identification frequencies. The result is available via the I 2 C-bus interface. A selection can be made via the I 2 C-bus for B/G, D/K and M standard and for three different modes that represent different trade-offs between speed and reliability of identification.

NICAM DEMODULATION

The NICAM signal is transmitted in a DQPSK code at a bit rate of 728 kbit/s. The NICAM demodulator performs DQPSK demodulation and feeds the resulting bitstream and clock signal onto the NICAM decoder and, for evaluation purposes, to PCLK (pin 1) and NICAM

(pin 2). A timing loop controls the frequency of the crystal oscillator to lock the sampling rate to the symbol timing of the NICAM data.

NICAM DECODER

The device performs all decoding functions in accordance with the “EBU NICAM 728 specification”. After locking to the frame alignment word, the data is descrambled by applying the defined pseudo-random binary sequence; the device will then synchronize to the periodic frame flag bit C0.

The status of the NICAM decoder can be read out from the NICAM status register by the user. The OSB bit indicates that the decoder has locked to the NICAM data. The VDSP bit indicates that the decoder has locked to the NICAM data and that the data is valid sound data. The C4 bit indicates that the sound conveyed by the FM mono channel is identical to the sound conveyed by the NICAM channel. The error byte contains the number of sound sample errors, resulting from parity checking, that occurred in the past 128 ms period.

NICAM AUTO-MUTE

This function is enabled by setting bit AMUTE LOW subaddress 14 Upper and lower error limits may be defined by writing appropriate values to two registers in the I 2 C-bus section (subaddresses 16 and 17; . When the number of errors in a 128 ms period exceeds the upper error limit the auto-mute function will switch the output sound from NICAM to whatever sound is on the first sound carrier (FM or AM). When the error count is smaller than the lower error limit the NICAM sound is restored. The auto-mute function can be disabled by setting bit AMUTE HIGH. In this condition clicks become audible when the error count increases; the user will hear a signal of degrading quality.

A decision to enable/disable the auto-muting is taken by the microcontroller based on an interpretation of the application control bits C1, C2, C3 and C4 and, possibly, any additional strategy implemented by the set maker in the microcontroller software.

For NICAM L applications, it is recommended to demodulate AM sound in the first sound IF and connect the audio signal to the mono input of the TDA9875A. By setting the AMSEL bit subaddress 14. the auto-mute function will switch to the audio ADC instead of switching to the first sound carrier.

CRYSTAL OSCILLATOR

The digital-controlled crystal oscillator (DCXO) is illustrated in Fig.8 (see Chapter 12). The circuitry of the DCXO is fully integrated, only the external 24.576 MHz crystal is needed.

TEST PINS

Both test pins are active HIGH, in normal operation of the device they are wired to VSSD1 Test functions are for manufacturing tests only and are not available to customers. Without external circuitry these pads are pulled down to LOW level with internal resistors.

POWER FAIL DETECTOR

The power fail detector monitors the internal power supply for the digital part of the device. If the supply has temporary been lower than the specified lower limit, the power-on reset bit POR, transmitter register subaddress 0 will be set to HIGH. The CLRPOR bit, slave register subaddress 1 resets the power-on reset flip-flop to LOW. If this is detected, an initialization of the TDA9875A has to be carried out to ensure reliable operation.

LEVEL SCALING

All input channels to the digital crossbar switch (except for the loudspeaker feedback path) are equipped with a level adjust facility to change the signal level in a range of 15 dB. It is recommended to scale all input channels to be 15 dB below full scale (15 dB full scale) under nominal conditions.

NICAM PATH

The NICAM path has a switchable J17 de-emphasis.

FM (AM) PATH

A high-pass filter suppresses DC offsets from the FM demodulator due to carrier frequency offsets and supplies the monitor/peak function with DC values and an unfiltered signal, e.g. for the purpose of carrier detection. The de-emphasis function offers fixed settings for the supported standards (50 μs, 60 μs 75 μs and J17). An adaptive de-emphasis is available for Wegener-Panda 1 encoded programs. A matrix performs the dematrixing of the A2 stereo, dual and mono signals.

NICAM AUTO-MUTE

If NICAM B/G, I, D/K is received, the auto-mute is enabled and the signal quality becomes poor, the digital crossbar switch switches automatically to FM and switches the matrix to channel 1. The automatic switching depends on the NICAM bit error rate.

The auto-mute function can be disabled via the I 2 C-bus. For NICAM L applications, it is recommended to demodulate AM sound in the first sound IF and connect the audio signal to the mono input of the TDA9875A. By setting the AMSEL bit subaddress 14 (see Section 10.3.11), the auto-mute function will switch to the audio ADC instead of switching to the

first sound carrier. The ADC source selector subaddress 23 (see Section 10.3.20) should be set to mono input, where the AM sound signal should be connected.

LOUDSPEAKER (MAIN) CHANNEL

The matrix provides the following functions; forced mono, stereo, channel swap, channel 1, channel 2 and spatial effects.

There are fixed coefficient sets for spatial settings of 30%, 40% and 52%.

The Automatic Volume Level (AVL) function provides a constant output level of 23 dB full scale for input levels between 0 and 29 dB full scale. There are some fixed decay time constants to choose from, i.e. 2, 4 and 8 seconds.

Pseudo stereo is based on a phase shift in one channel via a 2^{nd}-order all-pass filter. There are fixed coefficient sets to provide 90 degrees phase shift at frequencies of 150, 200 and 300 Hz.

Volume is controlled individually for each channel ranging from +24 to -83 dB with 1 dB resolution. There is also a mute position. For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I 2 C-bus data byte for volume control is identical to the volume setting in dBs (e.g. the I 2 C-bus data byte +10 sets the new volume value to +10 dB).

Balance can be realized by independent control of the left and right channel volume settings.

Contour is adjustable between 0 and +18 dB with 1 dB resolution. This function is linked to the volume setting by means of microcontroller software.

Bass is adjustable between +15 and -12 dB with 1 dB resolution and treble is adjustable between +/-12 dB with 1 dB resolution.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I 2 C-bus data byte for contour, bass or treble is identical to the new contour, bass or treble setting in dBs (e.g. the I 2 C-bus data byte +8 sets the new value to +8 dB). Extra bass boost is provided up to 20 dB with 2 dB resolution. The implemented coefficient set serves merely as an example on how to use this filter.

The beeper provides tones in a range from approximately 400 Hz to 30 kHz. The frequency can be selected via the I 2 C-bus. The beeper output signal is added to theloudspeaker and headphone channel signals. The beeper volume is adjustable with

respect to full scale between 0 and 93 dB with 3 dB resolution. The beeper is not effected by mute.

Soft-mute provides a mute ability in addition to volume control with a well defined time (32 ms) after which the soft-mute is completed. A smooth fading is achieved by a cosine masking.

HEADPHONE (AUXILIARY) CHANNEL

The matrix provides the following functions; forced mono, stereo, channel swap, channel and channel 2 (or C and S in Dolby Surround Pro Logic mode). Volume is controlled individually for each channel in a range from +24 to 83 dB with 1 dB resolution. There is also a mute position. For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I 2 C-bus data byte for volume control is identical to the volume setting in dB (e.g. the I 2 C-bus data byte +10 sets the new volume value to +10 dB). Balance can be realized by independent control of the left and right channel volume settings.

Bass is adjustable between +15 and -12 dB with 1 dB resolution and treble is adjustable between +/- 12 dB with 1 dB resolution.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I 2 C-bus data byte for bass or treble is identical to the new bass or treble setting in dB (e.g. the I 2 C-bus data byte +8 sets the new value to +8 dB).

The beeper provides tones in a range from approximately 400 Hz to 30 kHz. The frequency can be selected via the I 2 C-bus. The beeper output signal is added to the loudspeaker and headphone channel signals. The beeper volume is adjustable with respect to full scale between 0 and 93 dB with 3 dB resolution. The beeper is not effected by mute.

Soft-mute provides a mute ability in addition to volume control with a well defined time (32 ms) after which the soft-mute is completed. A smooth fading is achieved by a cosine masking.

SCART INPUTS

The SCART specification allows for a signal level of up to 2 V (rms). Because of signal handling limitations, due to the 5 V supply voltage of the TDA9875A, it is necessary to have fixed 3 dB attenuators at the SCART inputs to obtain a 2 V input. This results in a +3 dB SCART-to-SCART copy gain. If 0 dB copy gain is preferred (with maximum 1.4V input), there are +3 dB/0 dB amplifiers at the outputs of SCART 1 and SCART 2 and at the line

output. The input attenuator is realized by an external series resistor in combination with the input impedance, both of which form a voltage divider. With this voltage divider the maximum SCART signal level of 2 V (rms) is scaled down to 1.4 V (rms) at the input pin.

EXTERNAL AND MONO INPUTS

The 3 dB input attenuators are not required for the external and mono inputs, because those signal levels are under control of the TV designer. The maximum allowed input level is 1.4 V (rms). By adding external series resistors, the external inputs can be used as an additional SCART input.

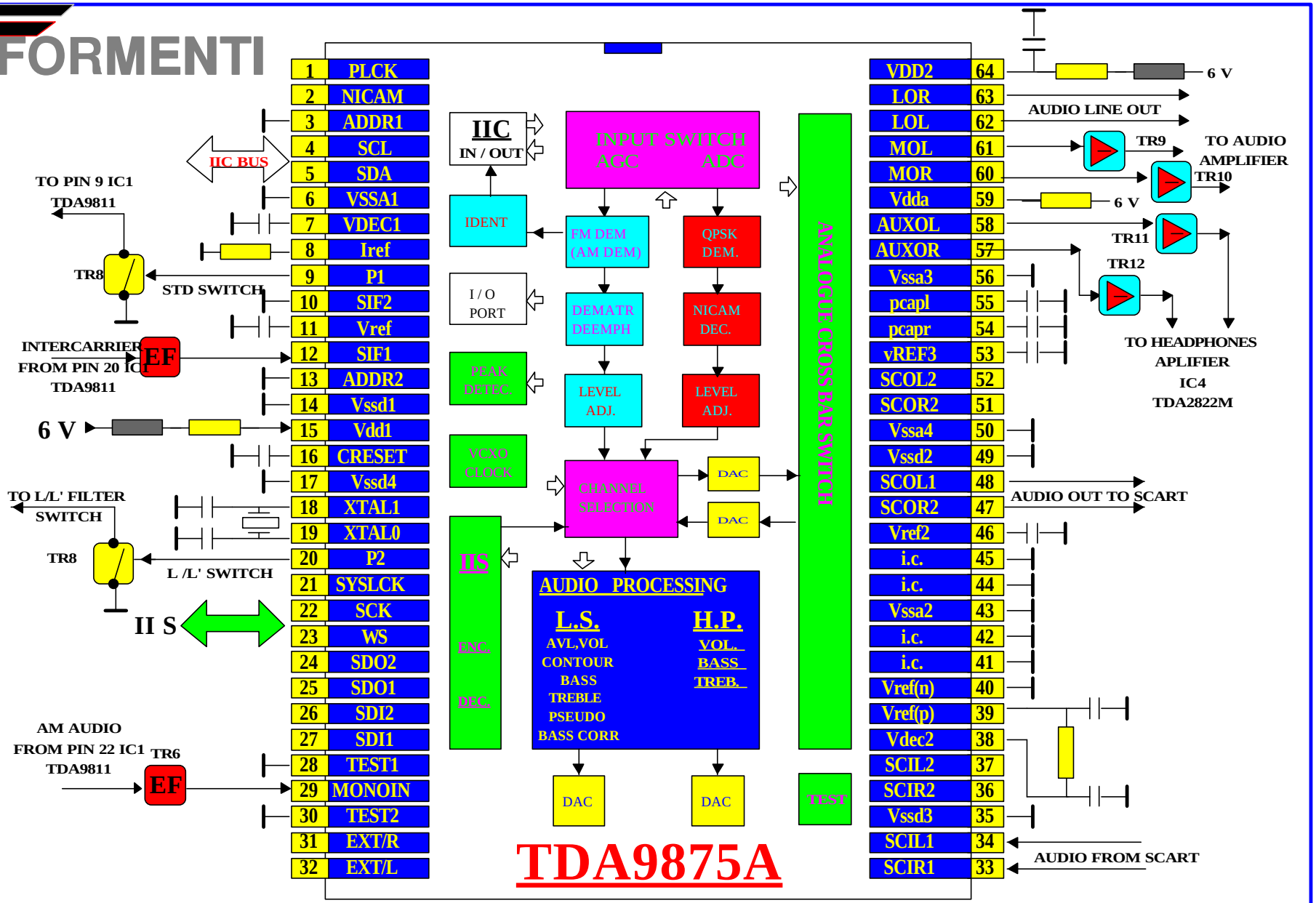
SCART OUTPUTS

The SCART outputs employ amplifiers with two gain settings. The gain can be set to +3 dB or to 0 dB via the I 2 C-bus. The +3 dB position is needed to compensate for the 3 dB attenuation at the SCART inputs should SCART-to-SCART copies with 0 dB gain be preferred [under the condition of 1.4 V (rms) maximum input level]. The 0 dB position is needed, for example, for an external-to-SCART copy with 0 dB gain.

LINE OUTPUT

The line output can provide an unprocessed copy of the audio signal in the loudspeaker channels. This can be either an external signal that comes from the dual audio ADC, or a signal from an internal digital audio source that comes from the dual audio DAC. The line output employs amplifiers with two gain settings. The +3 dB position is needed to compensate for the attenuation at the SCART inputs, while the 0 dB position is needed, for example, for non-attenuated external or internal digital signals (see Section 6.3.4).

FORMENTI



TDA9875A

TDA9875A PINOUT & PERIPHERALS

TDA9875A.DRW
E.G. 7/11/99

TDA9811

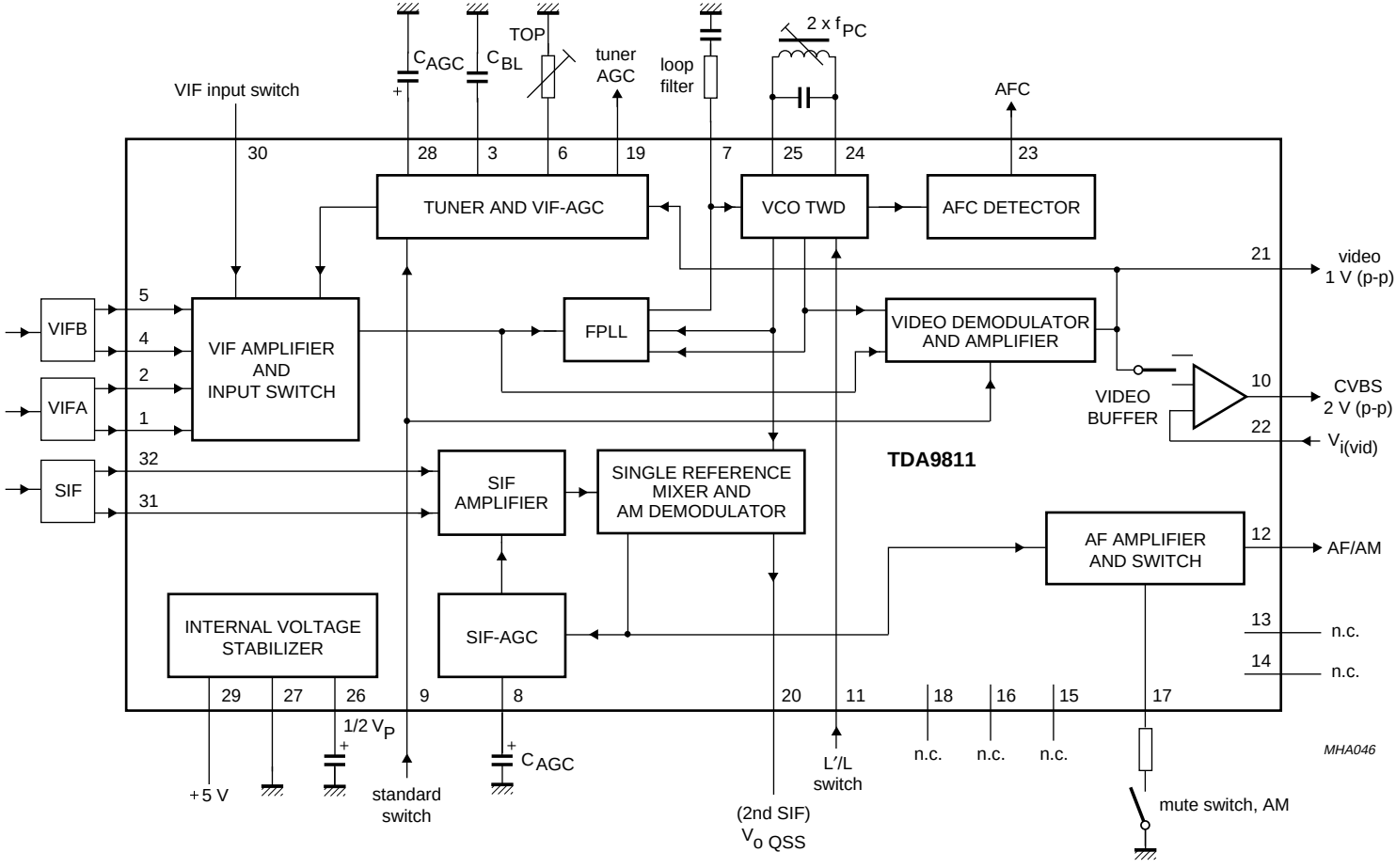
Multistandard VIF-PLL with QSS-IF and AM demodulator

FEATURES

- 5 V supply voltage
- Two switched VIF inputs, gain controlled wide band VIF-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Gated phase detector for L/L accent standard VCO frequency switchable between L and L accent (alignment external) picture carrier frequency
- Separate video amplifier for sound trap buffering with high video bandwidth VIF AGC detector for gain control, operating as peak sync detector for B/G (optional external AGC) and peak white detector for L; signal controlled reaction time for L
- Tuner AGC with adjustable takeover point (TOP)
- AFC detector without extra reference circuit
- SIF input for single reference QSS mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode
- AM demodulator without extra reference circuit
- AM mute (especially for NICAM)
- Stabilizer circuit for ripple rejection and to achieve constant output signals.

GENERAL DESCRIPTION

The TDA9811 is an integrated circuit for multistandard vision IF signal processing and sound AM demodulation, with single reference QSS-IF in TV and VCR sets.


VIF input switch
30
C_{AGC}
28
C_{BL}
3
TOP
6
tuner AGC
19
loop filter
7
2 x f_{PC}
25
24
AFC
23
TUNER AND VIF-AGC
VCO TWD
AFC DETECTOR
21
video 1 V (p-p)
VIFB
5
4
VIFA
2
1
VIF AMPLIFIER AND INPUT SWITCH
FPLL
VIDEO DEMODULATOR AND AMPLIFIER
VIDEO BUFFER
10
CVBS 2 V (p-p)
22
$V_{i(vid)}$
SIF
32
31
SIF AMPLIFIER
SINGLE REFERENCE MIXER AND AM DEMODULATOR
TDA9811
AF AMPLIFIER AND SWITCH
12
AF/AM
INTERNAL VOLTAGE STABILIZER
SIF-AGC
13
n.c.
14
n.c.
29
27
26
9
8
20
11
18
16
15
17
1/2 V_P
C_{AGC}
+5 V
standard switch
L′/L switch
n.c.
n.c.
n.c.
(2nd SIF) $V_{o\ QSS}$
mute switch, AM
MHA046

FUNCTIONAL DESCRIPTION

Vision IF amplifier and input switch The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitterdegeneration. T

The first differential stage is extended by two pairs of emitter followers to provide two IF input channels. The VIF input can be selected by pin 30

Tuner and VIF AGC

The AGC capacitor voltage is transferred to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current (open-collector output).

The tuner AGC takeover point can be adjusted. This allows the tuner and the SWIF filter to be matched to achieve the optimum IF input level.

The AGC detector charges/discharges the AGC capacitorto the required voltage for setting of VIF and tuner gain in order to keep the video signal at a constant level.

Therefore for negative video modulation the sync level and for positive video modulation the peak white level of the video signal is detected. In order to reduce the reaction time for positive modulation, where a very large time constant is needed, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step. The additional level information is given by the black-level detector voltage.

Frequency Phase Locked Loop detector (FPLL)

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier.

During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. The DC current of either frequency detector or phase detector is converted into a DC voltage via the loop filter, which controls the VCO frequency. In the event of positive modulated signals the phase detector is gated by composite sync in order to avoid signal distortion for overmodulated VIF signals.

VCO, Travelling Wave Divider (TWD) and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated variable capacitors.

The control voltage required to tune the VCO from its free-running frequency to actually double the PC frequency is generated by the frequency-phase detector and fed via the loop filter to the first variable capacitor (FPLL). This control voltage is amplified and additionally converted into a current which represents the AFC output signal. The VCO centre frequency can be decreased (required for L accent standard) by activating an additional internal capacitor. This is achieved by using the L accent switch. In this event the second variable capacitor can be controlled by a variable resistor at the L accent switch for setting the VCO centre frequency to the required L accent value. At centre frequency the AFC output current is equal to zero.

The oscillator signal is divided-by-two with a TWD which generates two differential output signals with a 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the 'in phase' signal of the travelling wave divider output. In the demodulator stage the video signal polarity can be switched in accordancewith the TV standard. The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics for B/G and L standard. The standard dependent level shift in this stage delivers the same sync level for positive and negative modulation. The video output signal is 1 V (p-p) for nominal vision IF modulation.

Video buffer

For an easy adaption of the sound traps an operational amplifier with internal feedback is used in the event of B/G and L standard. This amplifier is featured with a high bandwidth and 7 dB gain. The input impedance is adapted output stage delivers a nominal 2 V (p-p) positive video signal. Noise clipping is provided.

SIF amplifier and AGC

The sound IF amplifier consists of two AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration. The SIF AGC detector is related to the SIF input signals (average level of AM or FM carriers) and controls the SIF amplifier to provide a constant SIF signal to the AM demodulator and single reference QSS mixer. The SIF AGC reaction time is set to 'slow' for nominal video conditions. But with a decreasing VIF amplitude step the SIF AGC is set to 'fast' mode controlled by the VIF AGC detector. In FM mode this reaction time is also set to 'fast' controlled by the standard switch.

Single reference QSS mixer The single reference QSS mixer is realized by a multiplier.

The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO).

The mixer output signal is fed via a high-pass for attenuation of the video signal components to the output pin 20. With this system a high performance hi-fi stereo sound processing can be achieved.

AM demodulator

The AM demodulator is realized by a multiplier. The modulated SIF amplifier output signal is multiplied in phase with the limited (AM is removed) SIF amplifier output signal. The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the AF amplifier.

Internal voltage stabilizer and 1 ¤2 VP -reference

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

For all audio output signals the constant reference voltage cannot be used because large output signals are required.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF1}$	1	VIF differential input signal voltage 1
$V_{i\ VIF2}$	2	VIF differential input signal voltage 2
C_{BL}	3	black level detector
$V_{i\ VIF3}$	4	VIF differential input signal voltage 3
$V_{i\ VIF4}$	5	VIF differential input signal voltage 4
TADJ	6	tuner AGC takeover adjust (TOP)
T_{PLL}	7	PLL loop filter
C_{SAGC}	8	SIF AGC capacitor
STD	9	standard switch
$V_{o\ CVBS}$	10	CVBS output signal voltage
LSWI	11	L/L accent switch
$V_{o\ AF}$	12	AM audio voltage frequency output
n.c.	13	not connected
n.c.	14	not connected
n.c.	15	not connected
n.c.	16	not connected
MUTE	17	AM mute
n.c.	18	not connected
TAGC	19	tuner AGC output
$V_{o\ QSS}$	20	single reference QSS output voltage
$V_{o(vid)}$	21	composite video output voltage
$V_{i(vid)}$	22	video buffer input voltage
AFC	23	AFC output
VCO1	24	VCO1 reference circuit for $2f_{PC}$
VCO2	25	VCO2 reference circuit for $2f_{PC}$
C_{ref}	26	$\frac{1}{2}V_P$ reference capacitor
GND	27	ground
C_{VAGC}	28	VIF AGC capacitor
V_P	29	supply voltage
INSWI	30	VIF input switch
$V_{i\ SIF1}$	31	SIF differential input signal voltage 1
$V_{i\ SIF2}$	32	SIF differential input signal voltage 2

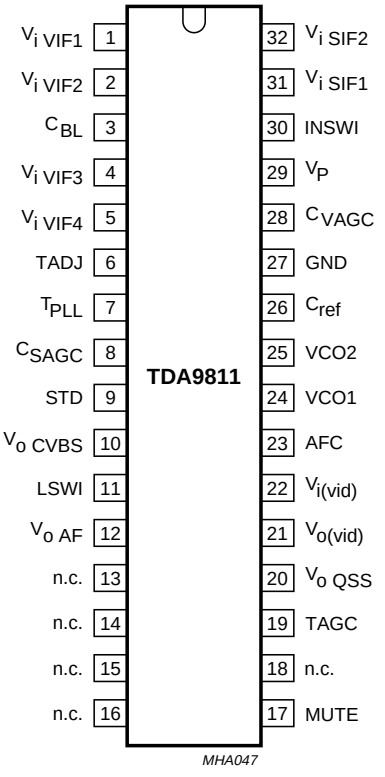


Fig.2 Pin configuration.

TDA9830

TV sound AM-demodulator and audio source switch

FEATURES

- Adjustment free wideband synchronous AM demodulator
- Audio source-mute switch (low noise)
- Audio level according EN50049
- 5 to 8 V power supply or 12 V alternative
- Low power consumption.

GENERAL DESCRIPTION

The TDA9830, a monolithic integrated circuit, is designed for AM-sound demodulation used in L- and L'-standard.
The IC provides an audio source selector and also mute switch.

FUNCTIONAL DESCRIPTION

Sound IF input

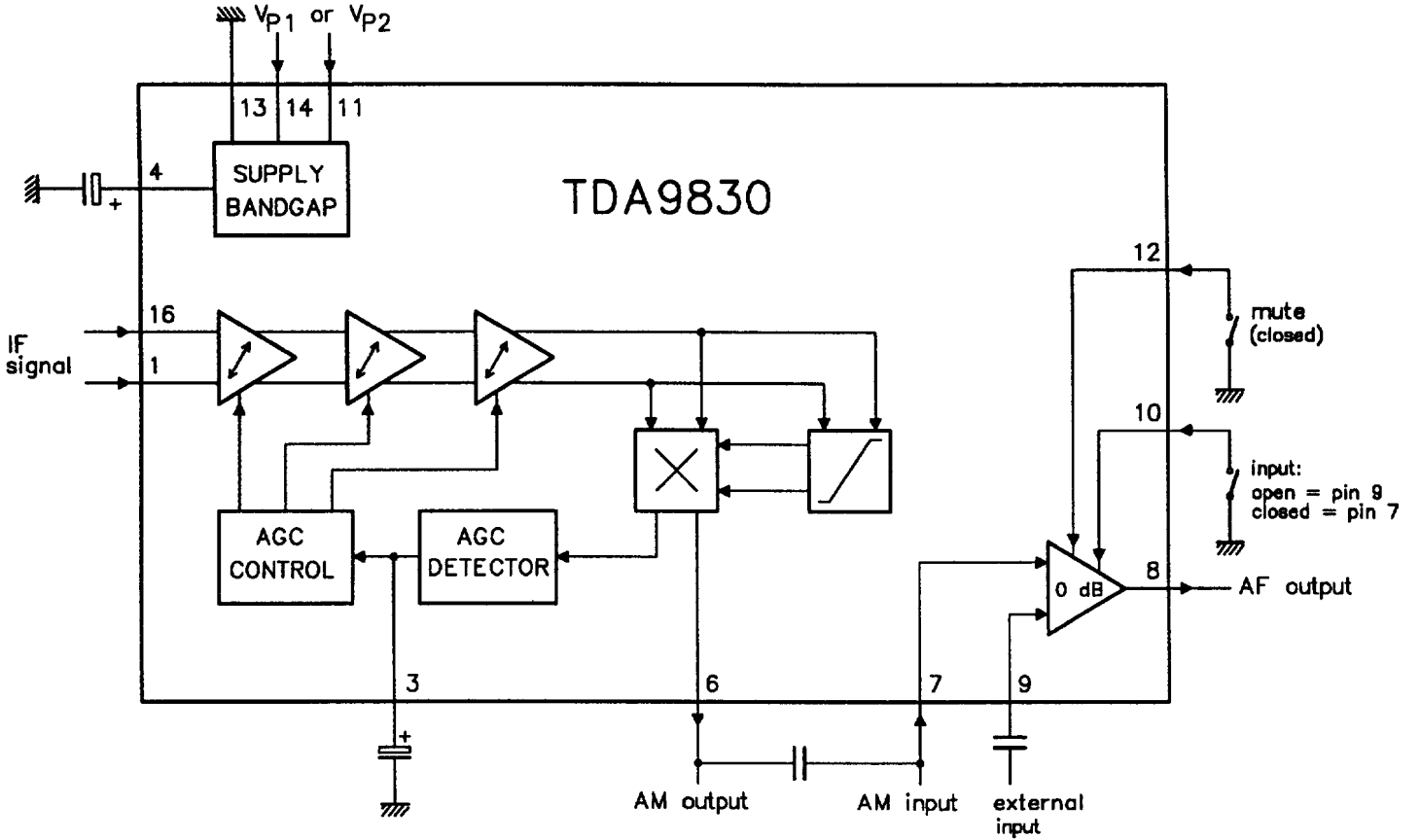
The sound IF amplifier consists of three AC-coupled differential amplifier stages each with approximately 20 dB gain. At the output of each stage is a multiplier for gain controlling ($\rightarrow$ current distribution gain control). The overall control range is approximately -6 to +60 dB and the frequency response (-3 dB) of the IF amplifier is approximately 6 to 70 MHz. The steepness of gain control is approximately 10 mV/dB.

IF AGC

The automatic gain control voltage to maintain the AM demodulator output signal at a constant level is generated by a mean level detector. This AGC-detector charges and discharges the capacitor at pin 3 controlled by the output signal of the AM-demodulator compared to an internal reference voltage. The maximum charge/discharge current is approximately 5 mA. This value in combination with the value of the AGC capacitor and the AGC steepness determines the lower cut-off audio frequency and the THD-figure at low modulation frequency of the whole AM-demodulator. Therefore a large time constant has to be chosen which leads to slow AGC reaction at IF level change. To speed up the AGC in case of IF signal jump from low to high level, there is an additional comparator built in, which can provide additional discharge current from the AGC capacitor up to 5 mA in a case of overloading the AM demodulator by the internal IF signal.

AM-demodulator

The IF amplifier output signal is fed to a limiting amplifier (two stages) and to a multiplier circuit. However the limiter output signal (which is not any more AM modulated) is also fed to the multiplier, which provides AM demodulation (in phase demodulation). After lowpass filtering ($f_g \approx 400$ kHz) for carrier rejection and buffering, the demodulator output signal is present at pin 6. The AM demodulator operates over a wide frequency range, so that in


V_{P1} or V_{P2}
13
14
11
4
SUPPLY BANDGAP
TDA9830
12
mute (closed)
16
IF signal
1
10
input: open = pin 9 closed = pin 7
AGC CONTROL
AGC DETECTOR
0 dB
8
AF output
3
6
7
9
AM output
AM input
external input

combination with the frequency response of the IF amplifier applications in a frequency range from approximately 6 MHz up to 70 MHz are possible.

Audio switch

This circuit is an operational amplifier with three input stages and internal feedback network determining gain (0 dB) and frequency response (fg ≈ 700 kHz). Two of the input stages are connected to pin 7 and pin 9, the third input stage to an internal reference voltage. Controlled by the switching pins 10 and 12, one of the three input stages can be activated and a choice made between two different AF signals or mute state. The selected signal is present at pin 8. The decoupling capacitors at the input pins are needed, because the internally generated bias voltage for the input stages must not be influenced by the application in order to avoid DC-plop in case of switching.

The AM demodulator output is designed to provide almost the same DC voltage as the input bias voltage of the audio switch. But there may be spread between both voltages.

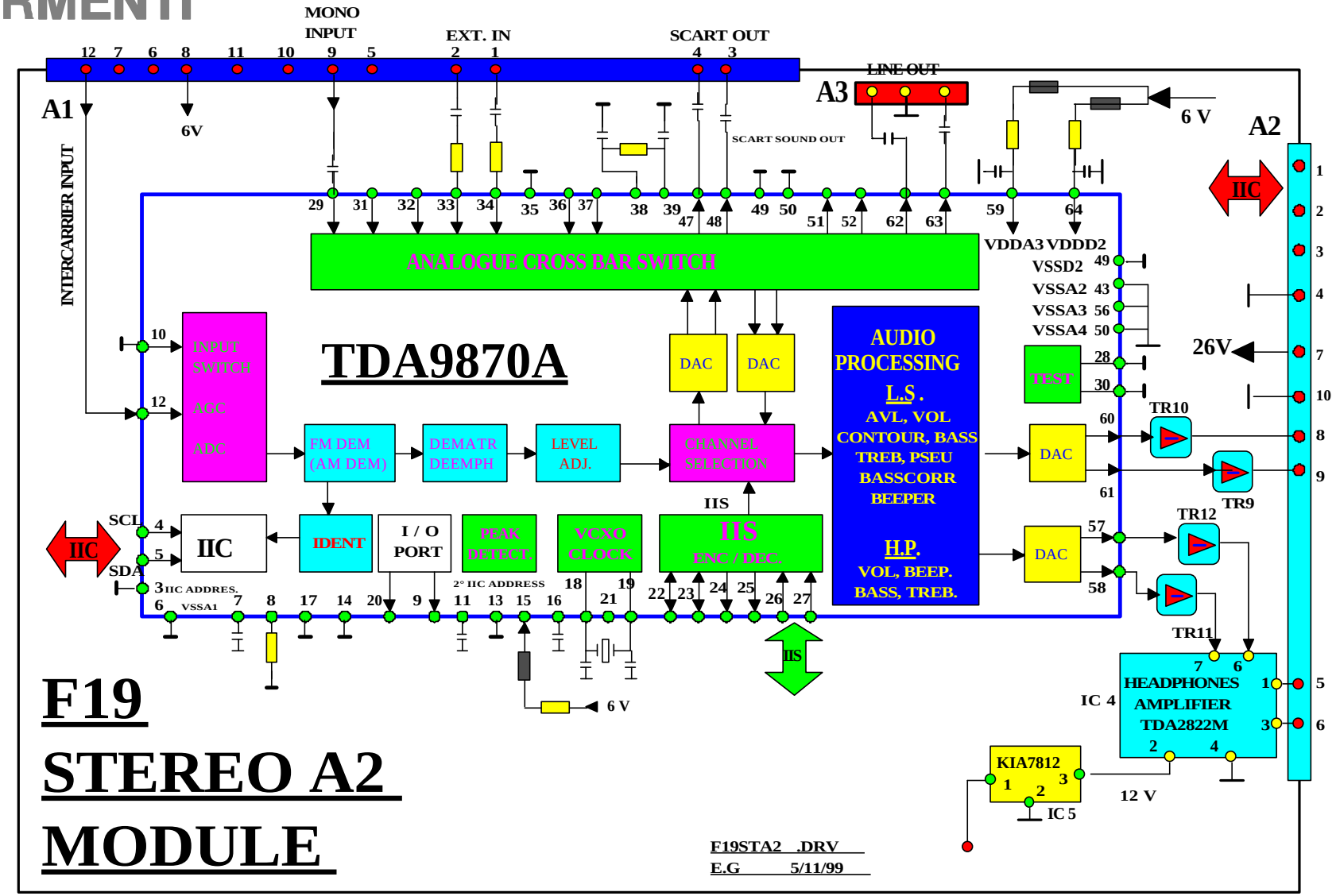
Therefore it is possible to connect pin 6 directly to pin 7 (without a decoupling capacitor), but in this event the DC-plop for switching can increase up to 100 mV.

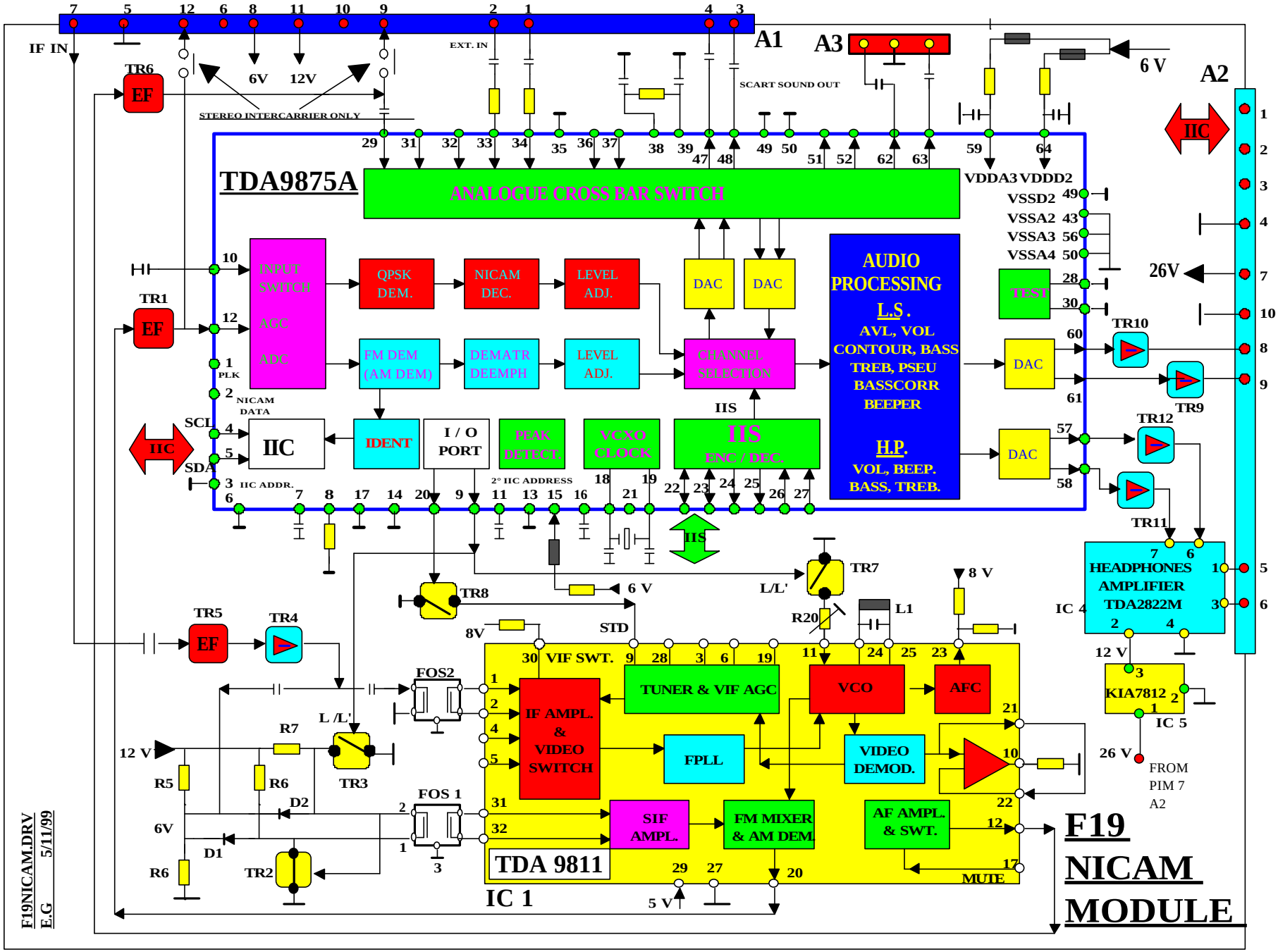
Reference circuit

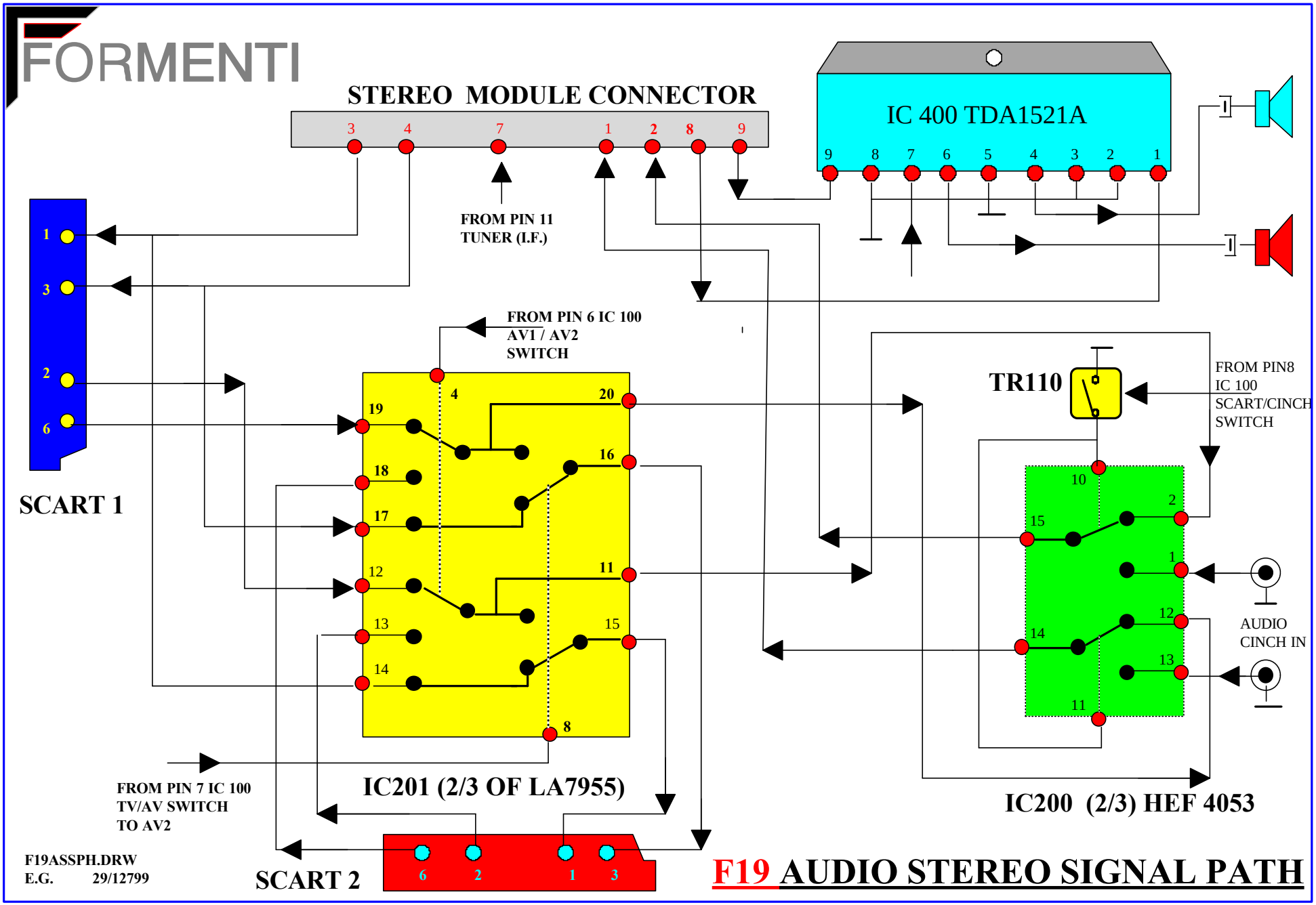
This circuit is a band gap stabilizer in combination with a voltage regulation amplifier, which provides an internal reference voltage of about 3.6 V nearly independent from supply voltage and temperature. This reference voltage is filtered by the capacitor at pin 4 in order to reduce noise. It is used as a reference to generate all important voltages and currents of the circuit. For application in 12 V power supply concepts, there is an internal voltage divider in combination with a Darlington transistor in order to reduce the supply voltage for all IC function blocks to approximately 6 V.

This is necessary because of use of modern high frequency IC technology, where most of the used integrated components are only allowed to operate at maximum 9 V supply voltage.

FORMENTI


MONO INPUT
EXT. IN
SCART OUT
LINE OUT
A1
A2
A3
6V
6 V
SCART SOUND OUT
INTERCARRIER INPUT
ANALOGUE CROSS BAR SWITCH
TDA9870A
INPUT SWITCH
AGC
ADC
FM DEM (AM DEM)
DEMATR DEEMPH
LEVEL ADJ.
CHANNEL SELECTION
DAC
DAC
AUDIO PROCESSING
L.S.
AVL, VOL
CONTOUR, BASS
TREB, PSEU
BASSCORR
BEEPER
H.P.
VOL, BEEP.
BASS, TREB.
TEST
DAC
DAC
DAC
IIC
SCL
SDA
IIC
IDENT
I / O PORT
PEAK DETECT
VCXO CLOCK
IIS
ENC / DEC.
IIS
IIC ADDRES.
2° IIC ADDRESS
VSSA1
VDDA3
VDDD2
VSSD2
VSSA2
VSSA3
VSSA4
26V
TR10
TR9
TR12
TR11
HEADPHONES AMPLIFIER TDA2822M
IC 4
KIA7812
IC 5
12 V
6 V
F19
STEREO A2
MODULE
F19STA2 .DRV
E.G 5/11/99


F19 NICAM MODULE
TDA9875A
ANALOGUE CROSS BAR SWITCH
AUDIO PROCESSING
L.S .
AVL, VOL
CONTOUR, BASS
TREB, PSEU
BASSCORR
BEEPER
H.P.
VOL, BEEP.
BASS, TREB.
INPUT SWITCH
AGC
ADC
QPSK DEM.
NICAM DEC.
LEVEL ADJ.
FM DEM (AM DEM)
DEMATR DEEMPH
CHANNEL SELECTION
DAC
TEST
IDENT
I / O PORT
PEAK DETECT.
VCXO CLOCK
IIS
ENC / DEC.
IIC
IF IN
EXT. IN
SCART SOUND OUT
STEREO INTERCARRIER ONLY
6V
12V
6 V
26V
8 V
8V
12 V
26 V
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
EF
R5
R6
R7
D1
D2
L1
R20
L /L'
FOS1
FOS2
IC 1
TDA 9811
IF AMPL. & VIDEO SWITCH
TUNER & VIF AGC
VCO
AFC
FPLL
VIDEO DEMOD.
SIF AMPL.
FM MIXER & AM DEM.
AF AMPL. & SWT.
MUTE
VIF SWT.
STD
IC 4
HEADPHONES AMPLIFIER TDA2822M
IC 5
KIA7812
FROM PIM 7 A2
A1
A2
A3
VDDA3 VDDD2
VSSD2
VSSA2
VSSA3
VSSA4
SCL
SDA
IIC ADDR.
2° IIC ADDRESS
NICAM DATA
PLK
F19NICAM.DRV
E.G 5/11/99


FORMENTI
STEREO MODULE CONNECTOR
3 4 7 1 2 8 9
IC 400 TDA1521A
9 8 7 6 5 4 3 2 1
FROM PIN 11
TUNER (I.F.)
1 3 2 6
SCART 1
FROM PIN 6 IC 100
AV1 / AV2
SWITCH
4 19 20 18 16 17 12 11 13 15 14 8
IC201 (2/3 OF LA7955)
TR110
FROM PIN8
IC 100
SCART/CINCH
SWITCH
10 2 15 1 12 14 13 11
AUDIO
CINCH IN
IC200 (2/3) HEF 4053
FROM PIN 7 IC 100
TV/AV SWITCH
TO AV2
6 2 1 3
SCART 2
F19ASSPH.DRW
E.G. 29/12799
F19 AUDIO STEREO SIGNAL PATH

FORMENTI

F 19

POWER SUPPLY

TDA4605

Control IC for Switched-Mode Power Supplies using MOS-Transistors

Features

- Fold-back characteristic provides overload protection for external components
- Burst operation under short-circuit conditions
- Loop error protection
- Switch-off if line voltage is too low (undervoltage switch-off)
- Line voltage compensation of overload point
- Soft-start for quiet start-up
- Chip-over temperature protection (thermal shutdown)
- On-chip parasitic transformer oscillation suppression circuitry

Functional desciption

The IC TDA 4605-1 controls the MOS-power transistor and performs all necessary regulation and monitoring functions in free running flyback converters. Since good load regulation over a wide load range is attained, this IC is applicable tor consumer and industrial power supplies.

The serial circuit of power transistor and primary winding of the flyback transformer is connected to the input voltage. During the switch - on period of the transistor, energy is stored in the transformer and during the switch - off period it is fed to the load via the secondary winding. By varying switch-ontime of the power transistor, the IC controls each portion of energy transferred to the secondary side such that the output voltage remains nearly independent ot load variations.

The required control information is taken from the input voltage during the switch-on period and from a regulation winding during the switch-off period.

In the different load ranges the switched-mode power supply (SMPS) behaves as follow:

No load operation:

The power supply unit oscillates at its resonant frequency typ. 100 kHz to 200 kHz. Depending upon
the transformator windings the output voltage can be slightly above nominal value.

Nominal operation:

The switching frequency declines with increasing load and decreasing AC-voltage. The duty factor primarly depends on the AC-voltage. The output voltage is load-dependent only.

Overload point:

Maximal output power is available at this point ot the output characteristic.

Overload:

The energy transferred per operation cycle is limited at the top. Therefore the output voltage declines by secondary overloading..Semiconductor Group 35

TDA 4605 Pin Definitions and Functions

Pin No. Function

1 Regulating Voltage: Information input concerning secondary voltage. By comparing the regulating voltage - obtained from the regulating winding ot the transformer - with the internal reference voltage, the output impulse width on pin 5is adapted to the load ot the secondary side (normal, overload, short-circuit, no load).

2 Primary Current Simulation: Information input regarding the primary current.

The primary current rise in the primary winding is simulated at pin 2 as a voltagerise by means ot external RC-element. When a value is reached that is derivedfrom the regulating voltage at pin 1, the output impulse at pin 5 is terminated. TheRC-element serves to set the maximum power at the overload point set.

3 Input for Primary Voltage Monitoring: In the normal operation V 3 is moving between the thresholds V 3H and V 3L (V 3H > V 3 > V 3L). V 3 < V 3L : SMPS is switched OFF (line voltage too low). V 3 > V 3H : Compensation of the overload point regulation (controlled by pin 2) starts at V 3H : V 3L = 1.7.

4 Ground

5 Output: Push-pull-output provides 1 A for rapid charge and discharge of the gate capacitance ot the power MOS-transistor.

5 Supply Voltage Input: A stable internal reference voltage *V* REF is derived from the supply voltage also the switching thresholds *V* 6A , *V* 6E , *V* 6 max and *V* 6 min for the supply voltage detector. If *V* 6 > *V* 6E then *V* REF is switched on and swiched off when *V* 6 < *V* 6A . In addition the logic is only enable for *V* 6 min < *V* 6 < *V* 6 max .

7 Soft-Start: Input for soft-start. Start-up will begin with short pulses by connecting a capacitor from pin 7 to ground.

8 Zero Detector: Input tor the oscillation feedback. After starting oscillation, every zero transit of the feedback voltage (falling edge) triggers an output impulse at pin 5. The trigger threshold is at + 50 mV typical..Semiconductor Group 36

TDA 4605 Application Circuit

Application circuit shows a flyback converter for video recorders with a power rating of 50 W. The circuit is designed as a wide-range power supply tor AC-line voltages ot 90 to 270 V. The AC-input voltage is rectified by bridge rectifier GR1 and smoothed by *C* 1 . The NTC limits the rush in current.In the period before the switch-on threshold is reached the IC is supplied via resistor *R* 1 ; during the start-up phase it uses the energy stored in *C* 2 , under steady-state conditions the IC receives its supply voltage from transformer winding *n* 1 via diode D1. The switching transistor T1 is a BUZ 90.

The parallel-connected capacitor *C* 3 and the inductance ot primary winding 112 determine the system resonance frequency. The *R* 2 - *C* 4 - D2 circuitry limits overshoot peaks, and *R* 3 protects the gate of T1 against static charges.

While T1 conducts, the current rise in the primary winding depends on the winding's inductance and the *V* C1 voltage. A voltage reproduction ot the current rise is tabbed using the *R* 4 - *C* 5 network and forwarded into pin 2 ot the IC. The RC-time constant ot *R* 4 , *R* 5 must be dimensioned correctly in order to prevent driving the transformer core into saturation.

The *R* 10 */R* 11 divider ratio provides the line voltage threshold controlling the undervoltage control circuit in the IC. The voltage present at pin 3 also determines the overload. Detection of overload together with the current characteristic at pin 2 controls the on period ot T1. This keeps the cut-off point stable even with higher AC-line voltages.

Pin 3 The down-divide primary voltage applied there stabilizes the overload point. In addition the logic is disabled in the event of low voltage by comparison with the internal stable voltage *V* V in the primary voltage monitor block.

Pin 4 Ground

Pin 5 In the output stage the output signals produced by the logic are shifted to a leved suitable for MOS-power transistors.

Pin 6 From the supply voltage *V* 6 are derived a stable internal reference *V* REF and the switching threshold *V* 6A , *V* 6E , *V* 6 max and *V* 6 min for the supply voltage monitor. All reference values *(V* R , *V* 2B , *V* ST) are derived from *V* REF . If *V* 6 > *V* VE the *V* REF is switched on and switched off when *V* 6 < *V* 6A . In addition, the logic is released only for *V* 6 min < *V* 6 < *V* 6 max .

Pin 7 The output of the overload amplifier is connected to pin 7. A load on this output causes a reductio in maximal impulse duration. This function can be used to implement a soft start, when pin 7 is connected to ground by a capacitor

Pin 8 The zero detector controlling the logic block recognizes the transformer being discharged by positive to negative zero crossing of pin 8 voltage and enables the logic for a new pulse. Parasitic oscillations occurring at the end of a pulse cannot lead to a new pulse (double-pulsing), because an internal circuit inhibits the zero detector for a finite time *t* UL after the end of each pulse.

Start-Up Behaviour

The start-up behaviour of the application circuit per sheet 48 is represented on sheet 50 for a line voltage barely above the lower acceptable limit voltage value (without soft-start). After applying the line voltage at the time *t* 0 to the tollowing voltages built up:

– *V* 6 corresponding to the half-wave charge current over *R* 1

– *V* 2 to *V* 2 max (typically 6.6 V)

– *V* 3 to the value determined by the divider *R* 10 */R* 11 .

The current drawn by the IC in this case is less than 1.6 mA. If *V* 6 reaches the threshold *V* 6E (time point *t* 1), the IC switches on the internal reference voltage. The currentdraw max. rises to 12 mA.

The primary current- voltage reproducer regulates *V* 2 down to *V* 2E and the starting impulse generator generates the starting impulses from time point *t* 5 to *t* 6 . The feedback to pin 8 starts the next impulse and so on. All impulses including the starting impulse are

controlled in width by regulating voltage of pin 1. When switching on this corresponds to a short-circuit event, i.e. *V* 1 = 0.

Hence the IC starts up with "short-circuit impulses" to assume a width depending on the regulating voltage feedback (the IC operates in the overload range). The maximum pulse width is reached at time point *t* 2 *(V* 2 = *V* 2 max). The IC operates at the overload point. Thereafter the peak values ot *V* 2 decrease rapidly, as the IC is operating within the regulation range. The regulating loop has built up. If voltage *V* 6 falls below the switch-off threshold *V* 6 min before the reversal point is reached, the starting attempt is aborted (pin 5 is switched to low). As the IC remains switched on, *V* 6 further decreases to *V* 6 . The IC switches off; *V* 6 can rise again (time point 14) and a new start-up attempt begins at time point *t* 1 . If the rectified alternating line voltage (primary voltage) collapses during load, *V* 3 can fall below *V* 3A , as is happening at time point *t* 3 (switch-on attempt when voltage is too low). The primary voltage monitor then clamps *V* 3 to *V* 3S until the IC switches off *(V* 6 < *V* 6A). Then a new start-up attempt begins at time point *t*

Regulation, Overload and No-Load Behaviour

When the IC has started up, it is operating in the regulation range. The potential at pin 1 typically is 400 mV. If the output is loaded, the regulation amplifier allows broader impulses *(V* 5 = H). The peak voltage value at pin 2 increases up to *V* 2S max . If the secondary load is further increased, the overload amplifier begins to regulate the pulse width downward. This point is referred to as the overload point of the power supply. As the IC supply voltage *V* 6 is directly proportional to the secondary voltage, it goes down in accordance with the overload regulation behaviour. If *V* 6 falls below the value *V* 6 min , the IC goes into burst operation. As the time constant of the half-wave charge-up is relatively large, the short-circuit power remains small. The overload amplifier cuts back to the pulse width *t* pk . This pulse width must remain possible, in order to permit the IC to start-up without problems from the virtual short circuit, which every switching on with *V* 1 = 0 represents. If the secondary side is unloaded, the loading impulses *(V* 5 = H) become shorter. The frequency increases up to the resonance frequency of the system. If the load is further reduced, the secondary voltages and *V* 6 increase. When *V* 6 = *V* 6 max , the logic is blocked. The IC converts to burst operation. This renders the circuit absolutely safe under no-load conditions.

Regulation of the switched-mode power supply is via pin 1. The control voltage of winding *n* 1 during the off-period of T1 is rectified by D3, smoothed by *C* 6 and stepped down at an adjustable ratio by *R* 5 , *R* 6 and *R* 7 . The *R* 6 - *C* 7 network suppresses parasitic overshoots (transformer oscillation).

The peak voltage at pin 2, and thus the primary peak current, is adjusted by the IC so that the voltage applied across the control winding, and hence the output voltages, are at the desired level.

When the transformer has supplied its energy to the load, the control voltage passes through zero.

The IC detects the zero crossing via series resistors *R* 9 connected to pin 8. But zero crossings are also produced by transformer oscillation after T1 has turned off if output is short-circuited. Thereforethe IC ignores zero crossings occurring within a specitied period of time after T1 turn-off.

The capacitor *C* 8 connected to pin 7 causes the power supply to be started with shorter pulses to keep the operating ftrequency outside the audible range during start-up.

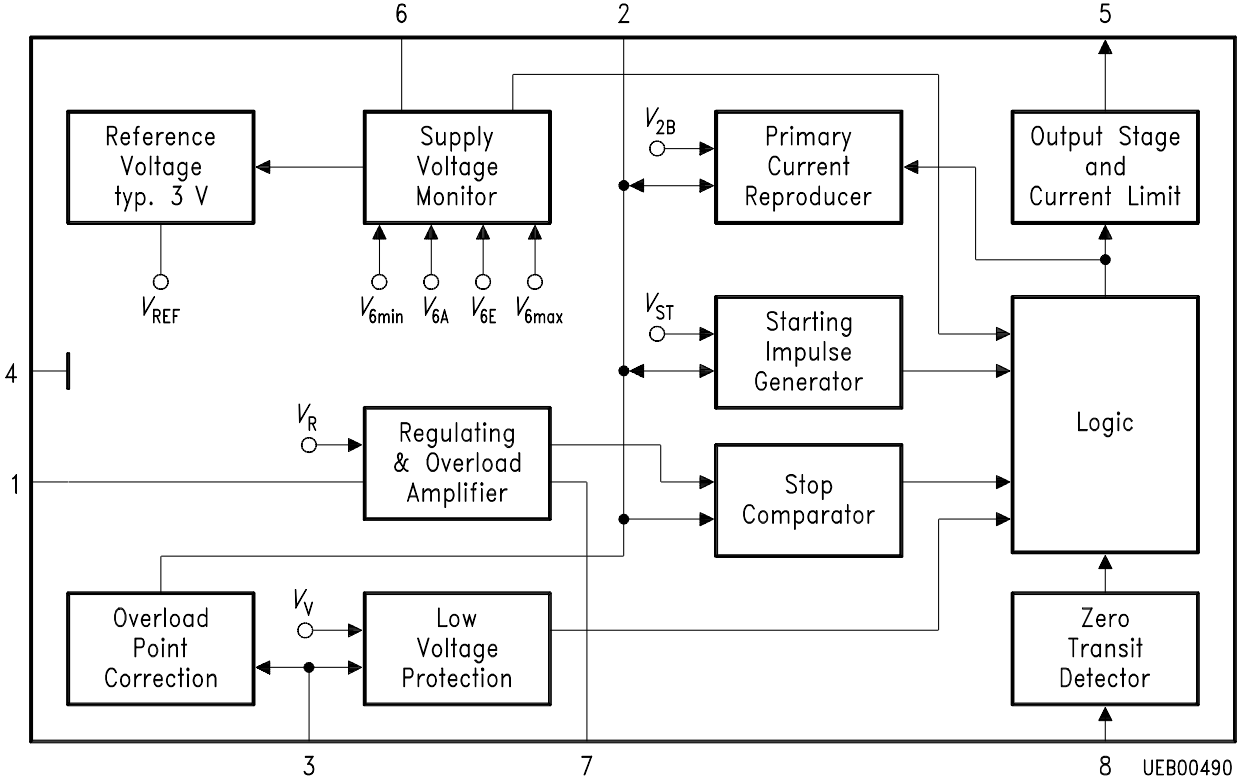
On the secondary side, tive output voltages are produced across winding *n* 3 to *n* 7 rectified by D4 to D8 and smoothed by *C* 9 to *C* 13 . Resistors *R* 12 , *R* 14 and *R* 19 to *R* 21 are used as bleeder resistors.

Fusable resistors *R* 15 to *R* 18 protect the rectifiers against short circuits in the output circuits, which are designed to supply only small loads..

TDA 4605 Block Diagram

Pin 1 The regulating voltage forwarded to this pin is compared with a stable internal reference voltage *V* R in the **regulating and overload amplifie**r. The output of this stage is ted to the stop comparator.

Pin 2 A voltage proportional to the drain current ot the switching transistor is generated there by theexternal RC-combination in conjunction with the **primary current transduce**r. The output of this transducer is controlled by the logic and referenced to the internal stable voltage *V* 2B . If the voltage *V* 2 exceeds the output voltage of the regulating amplifier, the logic is reset by the stop comparator and consequently the output ot pin 5 is switched to low potential. Further inputs tor the logic stage are the output for the **start impulse generator** with the stable reference potential *V* ST and the **supply voltage monito**r.

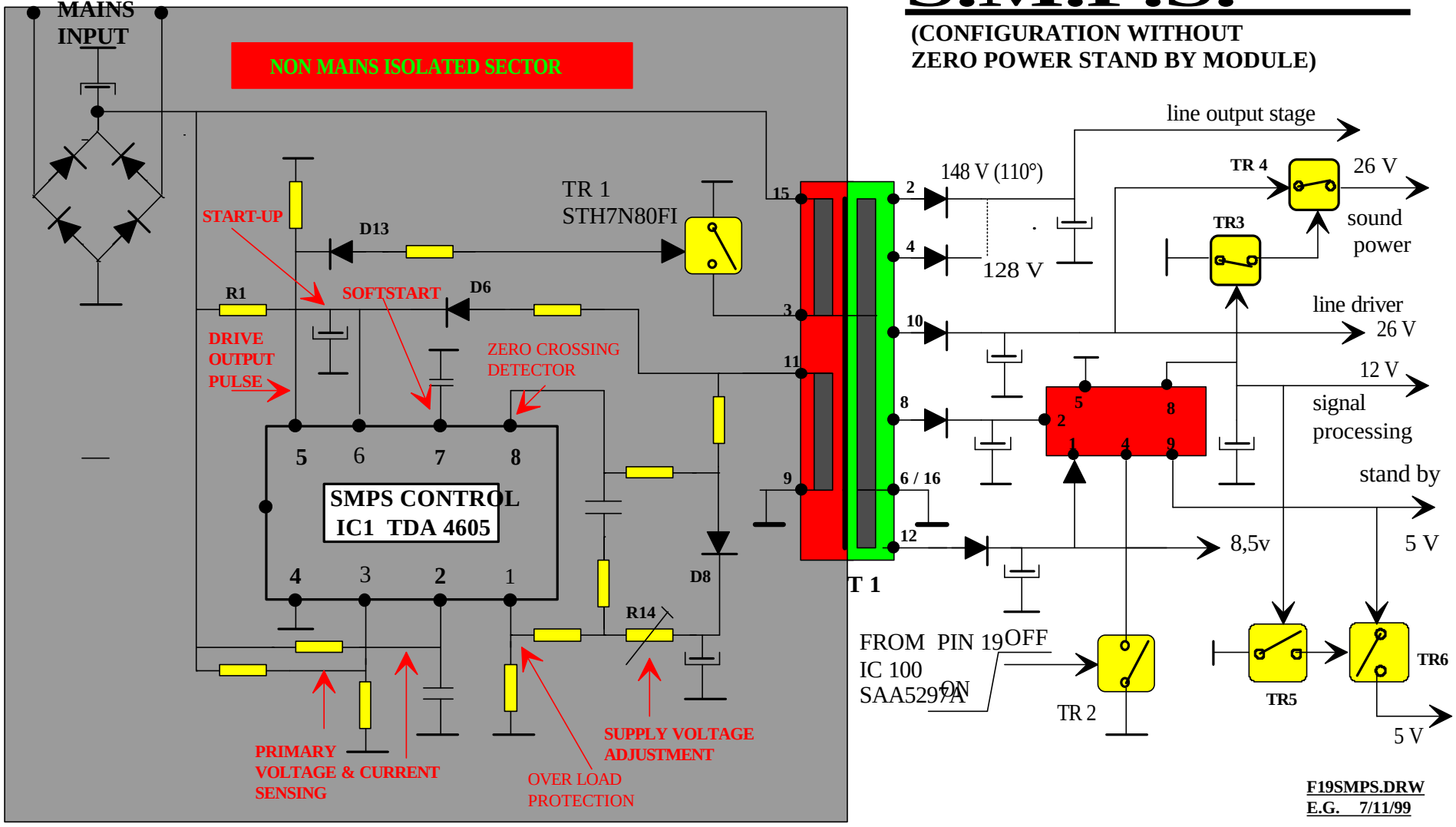

6
2
5
Reference Voltage typ. 3 V
Supply Voltage Monitor
V_{2B}
Primary Current Reproducer
Output Stage and Current Limit
V_{REF}
V_{6min}
V_{6A}
V_{6E}
V_{6max}
V_{ST}
Starting Impulse Generator
4
V_R
Regulating & Overload Amplifier
Logic
1
Stop Comparator
Overload Point Correction
V_V
Low Voltage Protection
Zero Transit Detector
3
7
8
UEB00490

FORMENTI

F 19

S.M.P.S.

(CONFIGURATION WITHOUT ZERO POWER STAND BY MODULE)



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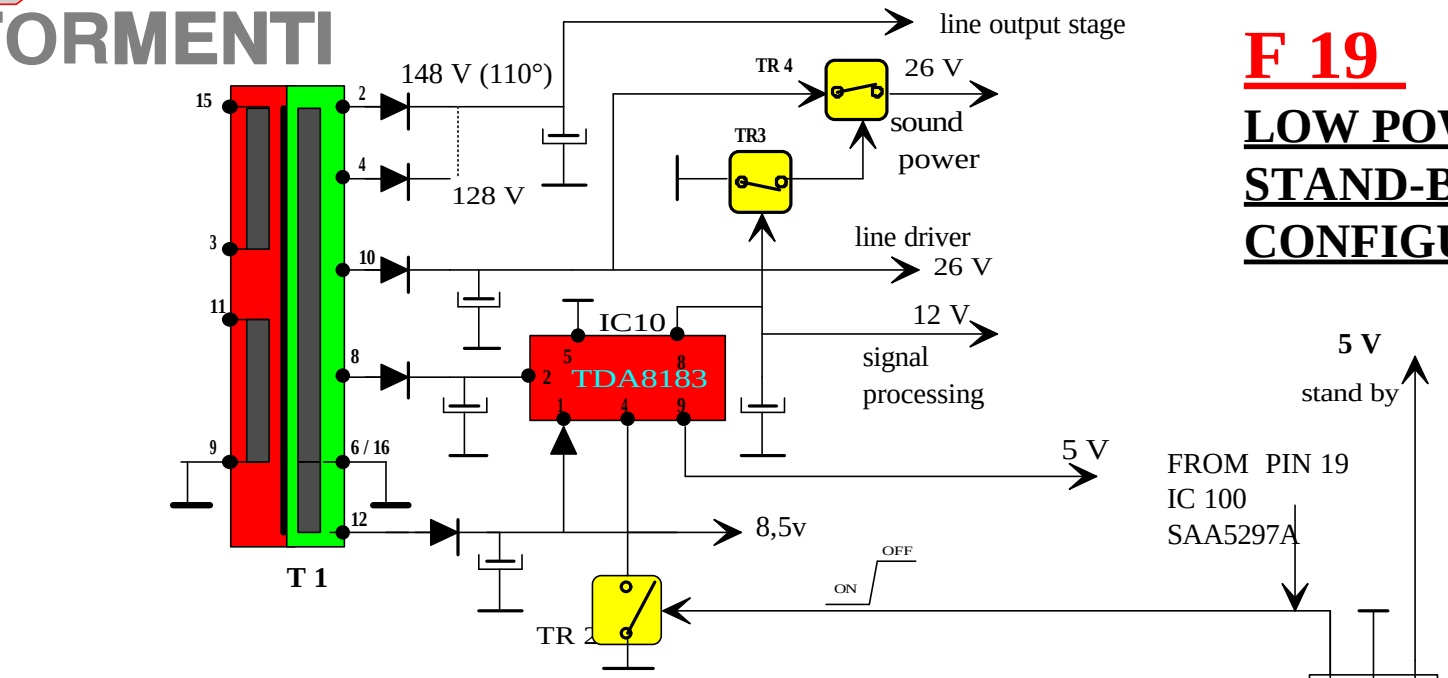
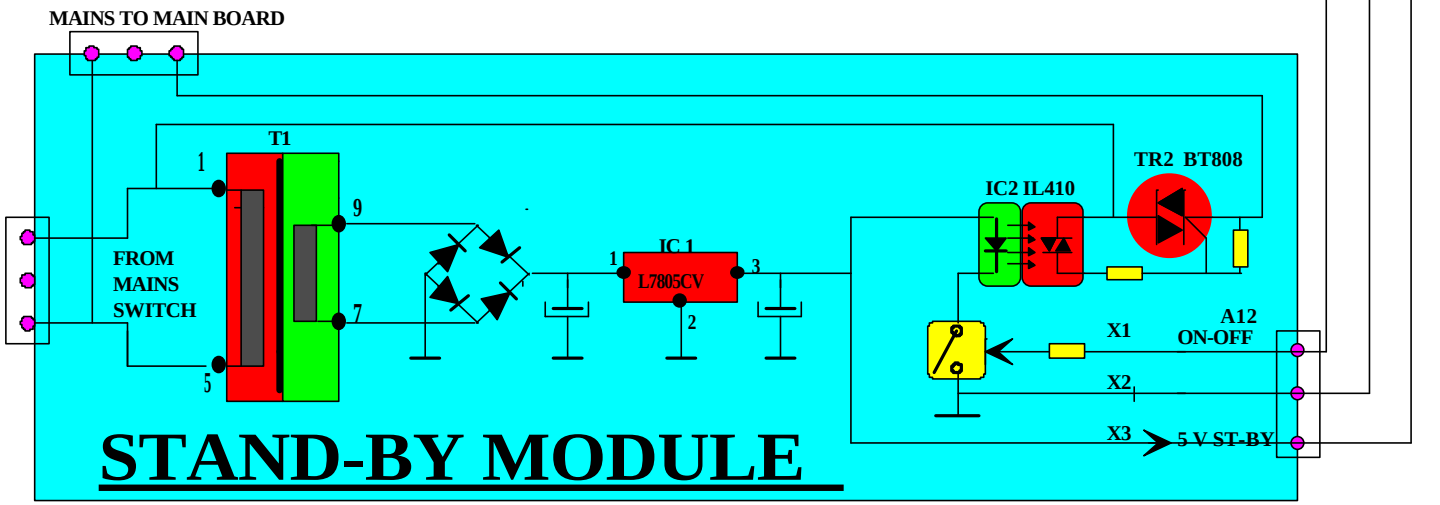
E.G. 7/11/99

FORMENTI

F 19

LOW POWER STAND-BY CONFIGURATION





STAND-BY MODULE

F19LPSBC.DRW
E.G. 14 /11/99

FORMENTI

F19
SERVICE MODE

F19 REMOTE CONTROL

For the description of the use of the TV make use of the Instruction Manual

Service mode

As already mentioned in the summary the remote control can be used to set all parameter and to adjust the TV set without to open the back cover.

There are two ways to enter the "SERVICE MODE" that are to use the LOCAL KEYBOARD or to have a precial prepared REMOTE CONTROL.

FIRST METHOD. (If the special remote control is available use the button following the indication of the Table 1

Table 1 List of command of the "SERVICE REMOTE CONTROL"

BUTTON	**RC5 Sub System**	**Decimal Coce**	**Function**
0	0	0	Vertical Slope
1	0	1	Vertical Amplitude
2	0	2	Vertical Shift
3	0	3	Vertical S Correctio
4	0	4	Horizontal Shift
5	0	5	HorizontalAmplitude
6	0	6	E-W parabola
7	0	7	E-W Corner
8	0	8	E-W Trapezium
9	0	9	AGC
Pr +	0	32	Up Carousel of all Service Parameter
Pr -	0	33	Down Carousel of all Service Parameter
Vol +	0	16	Adjust Parameter Value (UP)
Vol -	0	17	Adjust Parameter Value (Down)
TV	0	63	Leave SERVICE MODE" without to store
MEM	0	50	Leave SERVICE MODE with store
MENU	0	53	Wred
SERVICE	**7**	**58**	**SERVICE MODE ENTER**

Table 2 Parameter and value to be adjusted in "SERVICE MODE"

PARAMETER	VALUE	DESCRIPTION
init ctvfor v0.6	on/ off	Default Initialization
vg2test	on/off	Cut -off adjustment
txtbri	0--63	Adjust TXT brightness
txtcon	0--63	Adjust TXT Contrast
884c04	Bit (FSU)	Increase **blue stretch** and the **dynamic skin**
884c03	Bit (FSU)	Adj. **acl** (automatic colour limiter - and **cathode drive level**.
88c02	Bit (FSU)	Adj.(**black stretch**), **blue stretch**, and the **blue back**
optionb1	Bit (FSU)	Select TV standard and TXT character set
optionb2	Bit (FSU)	Scart type selections (
optionb3	Bit (FSU) (*)	Hotel mode setting
nicamuperror	0--63	Nicam sensitivity (upper limit)
nicamlowerror	0--63	Nicam sensitivity (Lower limit).
nicamcon	Bit (FSU)	Tda9875 CONTROL
pipcontrast	0--15	PIP Contrast control
wblue	0--63	Blue channel gain
wgreen	0--63	“Green channel gain
wred	0--63	“Red channel gain
ydelaypal	0--63	Luma chroma delay
ewtrapeze	0--63	E-W- Trapezium adjustment
ewcorner	0--63	E-W- Corner Adjustment
ewparab	0--63	E-W- Parabola Adjustment
ewwidth	0--63	Horizontal Amplitude
h-shift	0--63	Horizontal shift
s-corr	0--63	Vertical S-Correction
v-shift	0--63	Shift Vertical
v-ampl	0--63	Vertical Amplitude
v-slope	0--63	Slope Vertical
agc	0--63	AGC adjustment
if xx afc 2/3	0--63 (FSU)	Factory set up

LEGENDA: (FSU)= FACTORY SET UP (*) REDUCE OF A QUANITY 4 TO GET HOTEL MODE

WARNING!! Do not change value for those parameter that are highlighted please

Note 1

If during the installation of the TV set the AUTOSTORE" method is used, it is fundamental, before to start the function, to select the name of the country as the criteria of listing the broadcasters names is fixed by EBU table that are related to the country itself. It is possible to find more channels of the same broadcaster on the Arial. In this case the system will place first the signal having TXT with the strongest signal level than the others and finally, with the found sequence the weakest one without TXT.

Note 2

To get HOTEL MODE it is necessary to enter "SERVICE MODE" and to change the parameter "optionb3". Read the original value e subtract 4 (decimal). In HOTEL MODE all tuning systems are not possible, the volume is pre fixed and the MENU from the LOCAL KEY BOARD is not accessible.

Note 3

For fast programming (in case of installation of several TV set in Shops or Hotels a "Black Box" is available on request. The procedure for a quick program is as follows:

1. Install and tune all channel storing it in the program sequence you want
2. Switch off the Set with the remote control and leave it in Stand-by mode
3. Switch on the "Black Box" and connect it to Scart
4. Press the button corresponding to the chassis to be programmed and at the same time press the button "Read" for a while. (corresponding LED will be on.
5. When the LED "Write" became off (after few seconds) disconnect the "Black Box"
6. Insert the Black Box in the new TV set (in stand by condition)
7. Press F19 and "Write" buttons at same time. Corresponding "Write" LED will light
8. After few seconds when the "Write" LED will switch-off the procedure is finished .
9. Repeat points from 6 to 8 to program others TV set

WARNING!!!!! The above procedure can be applied only to TV set specially prepared for this functions

Table 4 List of languages that can be reproduced as a function of the TXT characters set setting with the optionb1 (bit number 6)

WEST EUROPE CHARACTER SET LANGUAGES	**EAST EUROPE CHARACTER SET LANGUAGES**
ENGLISH	POLISH
GERMAN	GERMAN
SWEDISH	ESTONIA
ITALIAN	SERB-CROAT
FRENCH	CZECH
SPANISH	RUMEN
TURKISH	

Just to give an example how to set the option byte 1, 2, and 3 we can start from a TV set for BG standard, with hyperband tuner to be sold in a country using West European character set.

Locking at the table 3 Optionb1 we have the following condition:

BIT	OPTIONB1			
NUMBER	0	1	VALUE	WEIGHT
0		BG	1	1
1		L/L'	0	
2		I	0	
3		DK	0	
4		X	0	
5		X	0	
6	E.E.TXT	W.E. TXT	1	64
7		CATV	1	128

Adding the value of the last column we get 193 in decimal form and C! in hexadecimal.
This means that we have to choose this value (C1) for the optionb1 in service mode

If we want to change from West Europe character set to East Europe, bit 6 became 0 that is the new value is 129 (128 plus 1)that in hexadecimal format is 41

REMEMBER TO INSERT COUNTRY TABLE

THE SECOND METHOD to enter service mode is to use the LOCAL KEY BOARD as describe here below

1. Starting from TV off press VOLUME + on the LOCAL KEYBOARD and in the mean time switch on the TV with the mains switch
2. Within three second switch on the TV using the **"SWITCH-OFF"** button on the **Remote Control**
3. A small windows with black background and yellow characters will appear in the middle of the screen.

PARAMETER VALUE

4. Using the Remote control, program + / - (top bottom) will change the "PARAMETER" and the VOLUME + / - (left / right) will change the value
5. Each parameter can be stored, leaving the service mode, by using the MEM (yellow) button on the remote control
6. To leave "SERVICE MODE" without to store the new value use the TV button.
7. It is not necessary to store each value one by one this means that you can change all value you need and finally leave the SERVICE MODE pressing the YELLOW button MEM.

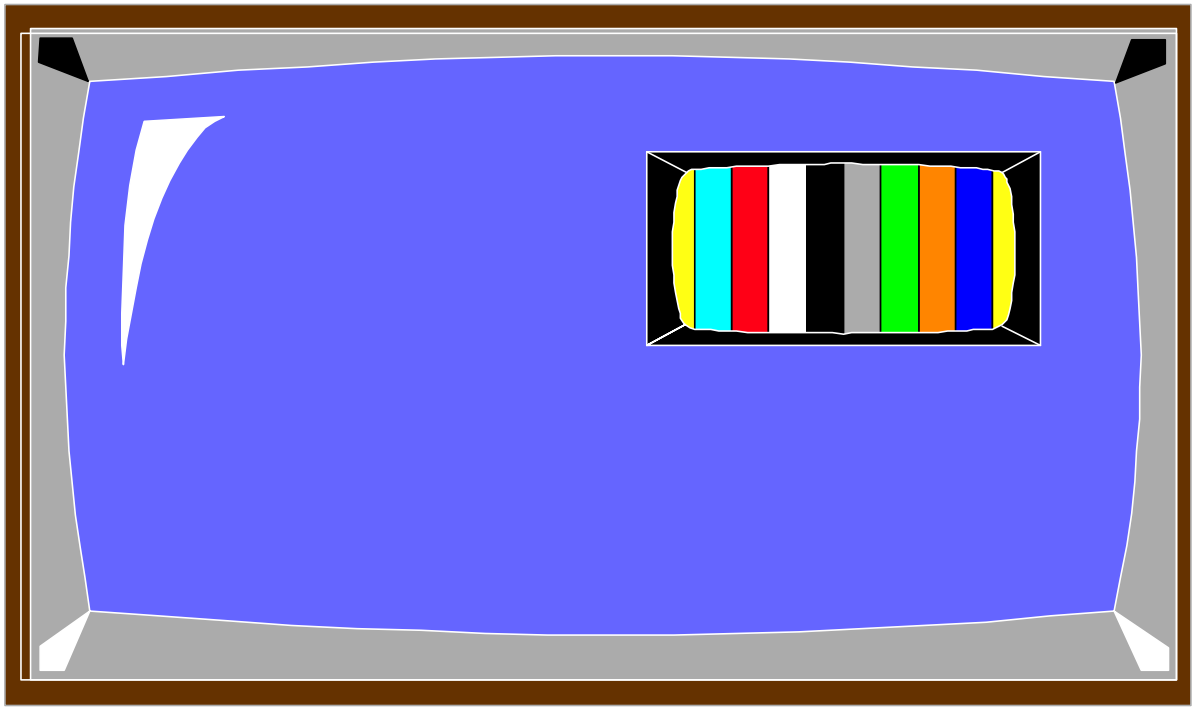
In the Table 3 we can find all parameter and related value to be seated. Some parameter have to adjusted with a simple on-off value, others are just factory option and more others must be adjusted with value that are expressed in hexadecimal form ranging from 0 to FF (that is from 0 to 63 in decimal form).

Table 3 represent the value to be assigned to three parameter to properly set options:

Table 3 Option bye (1, 2 and 3) value and related meaning

BIT	OPTIONB1		OPTIONB2		OPTIONB3	
WEIGHT	0	1	0	1	0	1
0		BG		2° SCART		FSU
1		L/L'		MUST BE 1		BACKGROUND
2		I		CINCH	HOTEL	
3		DK		SVHS		NTSC M
4		X		RGB		UV1316
5		X		X		V. GUARD
6	E.E.TXT	W.E.TXT		X		
7		CATV		X		

FORMENTI



PICTURE IN PICTURE MODULE

SDA 9288X

PICTURE IN PICTURE

1 General Description

The Picture-in-Picture Processor SDA 9288X A141 generates a picture of reduced size of a video signal (inset channel) for the purpose of combining it with another video signal (parent channel). The easy implementation of the IC in an existing system needs only a few additional external components. There is a great variety of application facilities professional and consumer products (TV sets, supervising monitors, multi-media, …)

Data Sheet

- 212 luminance and 53 chrominance pixels per inset line for picture size 1/9
- 6-bit amplitude resolution for each incoming signal component
- Field and frame mode display
- Horizontal and vertical filtering
- Special antialias filtering for the luminance signal

16:9 compatibility

- Operation in 4:3 and 16:9 sets
- 4:3 inset signals on 16:9 displays or v.v. with picture size 1/9 and 1/16, respectively

Analog inputs

- Y, + (B-Y), + (R-Y) or Y, -(B-Y), -(R-Y)

Analog outputs

- Y, + (B-Y), + (R-Y) or Y, – (B-Y), – (R-Y) or RGB
- 3 RGB matrices: EBU, NTSC (Japan), NTSC (USA)

Free programmable position of inset picture

- Steps of 1 pixel and 1 line
- All PIP and POP positions are possible

2 picture sizes

- 1/9 or 1/16 of normal size

High resolution display

13.5 MHz/27 MHz display clock frequency

Freeze picture

I 2 C Bus control

Threefold PIP/POP facility

- Three different I 2 C-addresses (pin-programmable)

System Description

AD Conversion, Inset Synchronization

The inset video signal is fed to the SDA 9288X A141 as analog luminance and chrominance components 1) . The polarity of the chrominance signals is programmable.

After clamping the video components are AD-converted with an amplitude resolution of 6 bit. The conversion is done using a 13.5 MHz clock for the luminance signal and a 3.375 MHz clock for the chrominance signals.

For the adaption to different application the clamp timing for the analog inputs can be chosen (CLPS; CLPFIX). Setting this bits to '1' can be useful for non-standard input signals.

For inset synchronization it is possible to feed either a special 3-level signal via pin HVI (detection of horizontal and vertical pulses) or separate signals via pins SCI for horizontal and VI for vertical synchronization. SCI is the horizontal synchron signal of the inset channel. If the burst gate pulse of the sandcastle is used it must be adapted to TTL compatible levels by a simple external circuit. Centering of the displayed picture area is possible by a programmable delay for the horizontal synchronization signal (HSIDEL).

The inset horizontal synchronization signals are sampled with 27 MHz. This 27 MHz clock and the AD converter clocks are derived from the parent horizontal synchronization pulse or from the quartz frequency converted by a factor of 4/3.

Delay differences between luminance and chrominance signals at the input of the IC caused by chroma decoding are compensated by a programmable luminance delay line (YDEL) of about – 290 ns … 740 ns (at decimation input

By analyzing the synchronization pulses the line standard of the inset signal source is detected and interference noise on the vertical sync signal is removed. For applications with fixed line standard (only 625 lines or 525 lines) the automatic detection can be switched off.

The phase of the vertical sync pulse is programmable (VSIDEL; VSPDEL). By this way a correct detection of the field number is possible, an important condition for frame mode display.

Input Signal Processing

This stage performs the decimation of the inset signal by horizontal and vertical filtering and sub-sampling. A special antialias filter improves the frequency response of the luminance channel. It is optimized for the use of the horizontal decimation factor 3:1.
A window signal, derived from the sync pulses and the detected line standard, defines the part of the active video area used for decimation. For HSIDEL = '0' the decimation window is opened about 104 clock periods (13.5 MHz) after the horizontal synchronization pulse. For the 625 lines standard the 36th video line is the first decimated line, for the 525 lines standard decimation starts in the 26th video line.
The realized chrominance filtering allows omitting the color decoder delay line for PAL and SECAM demodulation if the color decoder supplies the same output voltages independent of the kind of operation. In case of SECAM signals an amplification of the chrominance signals by a factor of 2 is necessary because just every second line a signal is present. This chrominance amplification is programmable via pin SYS or I 2 C Bus (AMSEC). The horizontal and vertical decimation factors are free programmable (DECHOR, DECVER). Using different decimations horizontal and vertical 16:9 applications become realizable: DECHOR = '1', DECVER = '0': picture size 1/9 for 4:3 inset signals on 16:9 displays DECHOR = '0', DECVER = '1': picture size 1/16 for 16:9 inset signals on 4:3 displays

PIP Field Memory

The on-chip memory stores one decimated field of the inset picture. Its capacity is 169 812 bits. The picture size depends on the horizontal and vertical decimation factors.
In field mode display just every second inset field is written into the memory, in frame mode display the memory is continuously written. Data are written with the lower inset clock frequency depending on the horizontal decimation factor (4.5 MHz or 3.375 MHz).
Normally the read frequency is 13.5 MHz and 27 MHz for scan conversion systems.
For progressive scan conversion systems and HDTV displays a line doubling mode is available (LINEDBL). Every line of the inset picture is read twice. Memory writing can be stopped by program (FREEZE), a freeze picture display results (one field).
Having no scan conversion and the same line numbers in inset and parent channel (625 lines or 525 lines both) frame mode display is possible. The result is a higher vertical and time resolution because of displaying every incoming field. For this purpose the standards are internally analysed and activating of frame mode display is blocked automatically when the described restrictions are not fulfilled.
As in the inset channel a field number detection is carried out for the parent channel.

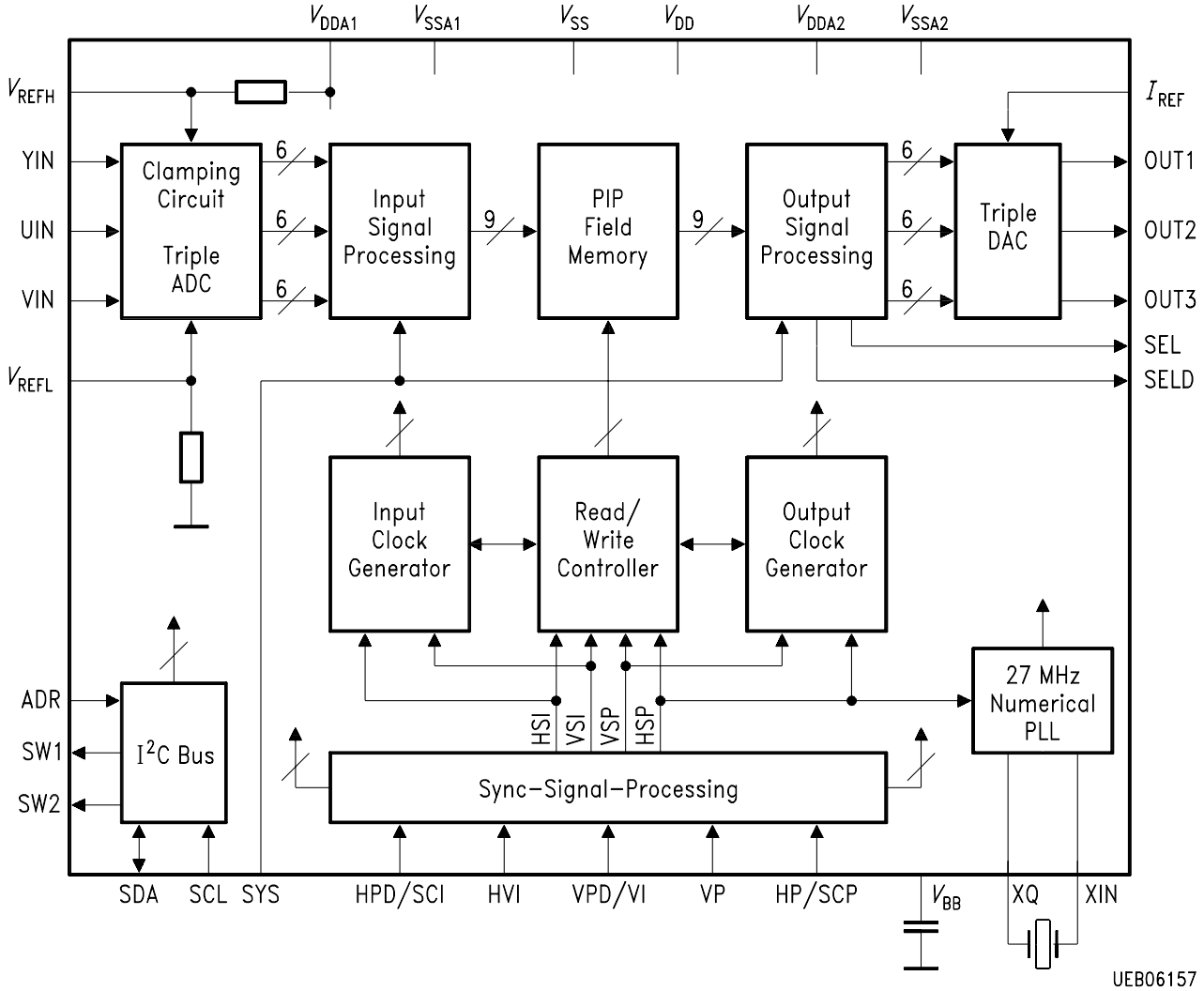
Depending on the phase between inset and parent signals a correction of the display raster for the read out data is performed by omitting or inserting lines when the read address counter outruns the write address counter.
The display position of the inset picture is free programmable (POSHOR, POSVER).
The first possible picture position (without frame) is 54 clock periods (13.5 MHz or 27 MHz) after the horizontal and 4 lines after the vertical synchronization pulses. Starting at this position the picture can be moved over the whole display area. Even POP-positions (Picture Outside Picture) at 16:9 applications are possible.

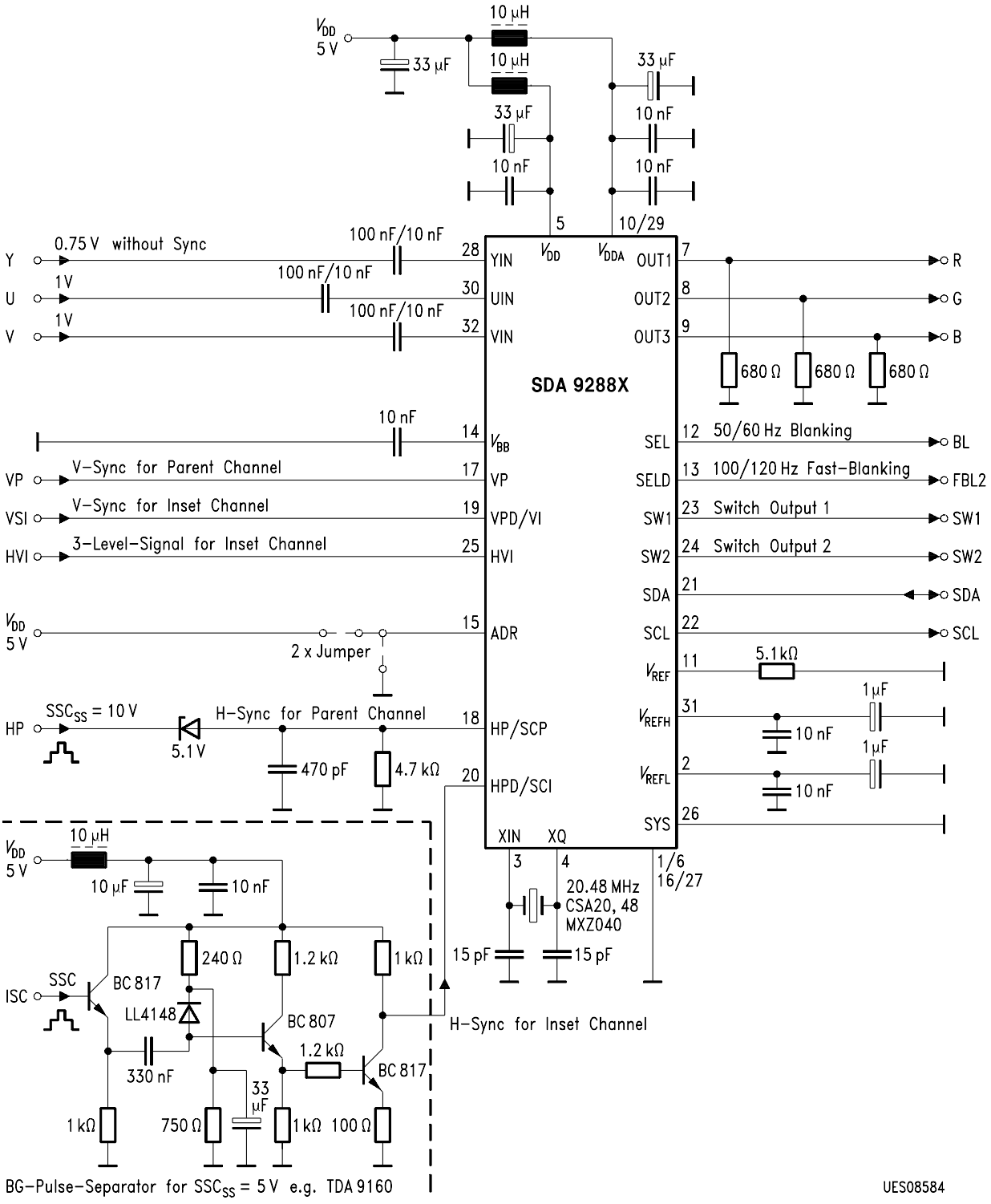
Horizontal Decimation PIP PIXELS per Line

Having different line standards in inset and parent channels we have a so called mixed mode display. It causes deformations in the aspect ratio of the inset picture. A special mixed mode display is available for the picture size 1/9 (MIXDIS):
Synchronization of memory reading with the parent channel is achieved by processing the parent horizontal and vertical synchronization signals in the same way as described for the inset channel. The synchronization signals are fed to the IC at pin HP/SCP for horizontal synchronization and pin VP for vertical synchronization. In the same way as described for the inset channel the burst gate of the sandcastle signal can be used for horizontal synchronization. In scan conversion systems also the inputs HPD/SCI and VPD/VI are available if the input HVI is activated for inset synchronization.

2.4 Output Signal Processing

At the memory output the chrominance components are demultiplexed and linearly interpolated to the luminance sample rate. Different output formats are available: luminance signal Y with inverted or non-inverted chrominance signals (B-Y), (R-Y) or RGB. For the RGB conversion 3 matrices are integrated: Matrix selection is done by pin SYS or I 2 C Bus. The matrices are designed for the following input voltages (100 % white, 75 % color saturation):


V_{DDA1}
V_{SSA1}
V_{SS}
V_{DD}
V_{DDA2}
V_{SSA2}
V_{REFH}
I_{REF}
YIN
UIN
VIN
Clamping Circuit
Triple ADC
6
6
6
Input Signal Processing
9
PIP Field Memory
9
Output Signal Processing
6
6
6
Triple DAC
OUT1
OUT2
OUT3
SEL
SELD
V_{REFL}
Input Clock Generator
Read/ Write Controller
Output Clock Generator
ADR
SW1
SW2
I^2C Bus
HSI
VSI
VSP
HSP
Sync–Signal–Processing
27 MHz Numerical PLL
SDA
SCL
SYS
HPD/SCI
HVI
VPD/VI
VP
HP/SCP
V_{BB}
XQ
XIN
UEB06157


SDA 9288X
V_{DD} 5 V
10 µH
33 µF
10 nF
5
10/29
0.75 V without Sync
1 V
100 nF/10 nF
Y
U
V
28 YIN
30 UIN
32 VIN
V_{DD}
V_{DDA}
OUT1 7
OUT2 8
OUT3 9
R
G
B
680 Ω
14 V_{BB}
VP
17 VP
V-Sync for Parent Channel
VSI
19 VPD/VI
V-Sync for Inset Channel
HVI
25 HVI
3-Level-Signal for Inset Channel
15 ADR
2 x Jumper
HP
SSC_{SS} = 10 V
5.1 V
H-Sync for Parent Channel
18 HP/SCP
470 pF
4.7 kΩ
20 HPD/SCI
SEL 12 50/60 Hz Blanking
BL
SELD 13 100/120 Hz Fast-Blanking
FBL2
SW1 23 Switch Output 1
SW2 24 Switch Output 2
SDA 21
SCL 22
V_{REF} 11
5.1 kΩ
V_{REFH} 31
V_{REFL} 2
1 µF
SYS 26
XIN 3
XQ 4
1/6
16/27
20.48 MHz
CSA20, 48
MXZ040
15 pF
ISC
SSC
BC 817
LL4148
BC 807
240 Ω
1.2 kΩ
1 kΩ
330 nF
33 µF
750 Ω
100 Ω
H-Sync for Inset Channel
BG-Pulse-Separator for SSC_{SS} = 5 V e.g. TDA 9160
UES08584

TDA8310A

PAL/NTSC colour processor for PIP applications

FEATURES

- Video switch with 2 CVBS inputs. One input can beswitched between CVBS and Y/C and the circuit can automatically detect whether the incoming signal is CVBS or Y/C
- Integrated chrominance trap and bandpass filters (automatically calibrated)
- Integrated luminance delay line
- Automatic PAL/NTSC decoder which can decode all standards available in the world
- Easy interfacing with the TDA8395 (SECAM decoder) for multistandard applications
- Horizontal PLL with an alignment-free horizontal oscillator
- Vertical count-down circuit
- RGB/YUV and fast blanking switch with 3-state output and active clamping
- Low dissipation (560 mW)
- Small amount of peripheral components compared with competition Ics

GENERAL DESCRIPTION

The TDA8310A is an alignment-free PAL/NTSC colour processor for Picture-in-Picture (PIP) applications.
The main difference between the TDA8310 and the TDA8310A is that the vision IF amplifier has been omitted in the TDA8310A. Therefore, the circuit contains an input signal selector, a PAL/NTSC colour decoder, horizontal and vertical synchronization and an RGB/YUV switch.
The input signal selector has 2 CVBS inputs. One of the inputs can be switched between CVBS and Y/C and the circuit can automatically detect whether the incoming signal is CVBS or Y/C. The output signals for the PIP processor are:

- Luminance signal
- Colour difference signals (U and V)
- Horizontal and vertical synchronization pulses.
- The RGB/YUV switch can select between two RGB or YUV sources, e.g. between the PIP processor and the SCART input signal.
- The supply voltage for the IC is 8 V. It is available in a 52-pin SDIP package.

FUNCTIONAL DESCRIPTION

CVBS switch

The circuit contains a 2 input CVBS switch and one of the inputs can be switched between CVBS and Y/C.
The circuit contains an identification circuit which can automatically switch between the CVBS and Y/C signals.
It is also possible to force the switch to CVBS or Y/C.

Synchronization circuit

The sync separator is preceded by a voltage controlled amplifier which adjusts the sync pulse amplitude to a fixed level. The sync pulses are fed to the slicing stage (separator) which operates at 50% of the amplitude.
The separated sync pulses are fed to the first phase detector and to the coincidence detector. The coincidence detector is used to detect whether the line oscillator is synchronized and for transmitter identification. The first PLL has a very high static steepness this ensures that the phase of the picture is independent of the line frequency.
The line oscillator operates at twice the line frequency. The oscillator network is internal. Because of the spread of internal components an automatic adjustment circuit has been added to the IC.
The circuit compares the oscillator frequency with that of the crystal oscillator in the colour decoder. This results in a free-running frequency which deviates less than 2% from the typical value.
The horizontal output pulse is derived from the horizontal oscillator via a pulse shaper. The pulse width of the output pulse is 5.4 ms, the front edge of this pulse coincides with the front edge of the sync pulse at the input.
The vertical output pulse is generated by a count-down circuit. The pulse width is approximately 380 ms. Both the horizontal and vertical output pulses will always be available at the outputs even when no input signal is available. In addition to the horizontal and vertical sync pulse outputs
the IC has a sandcastle pulse output which contains burst key and blanking pulses.

Integrated video filters

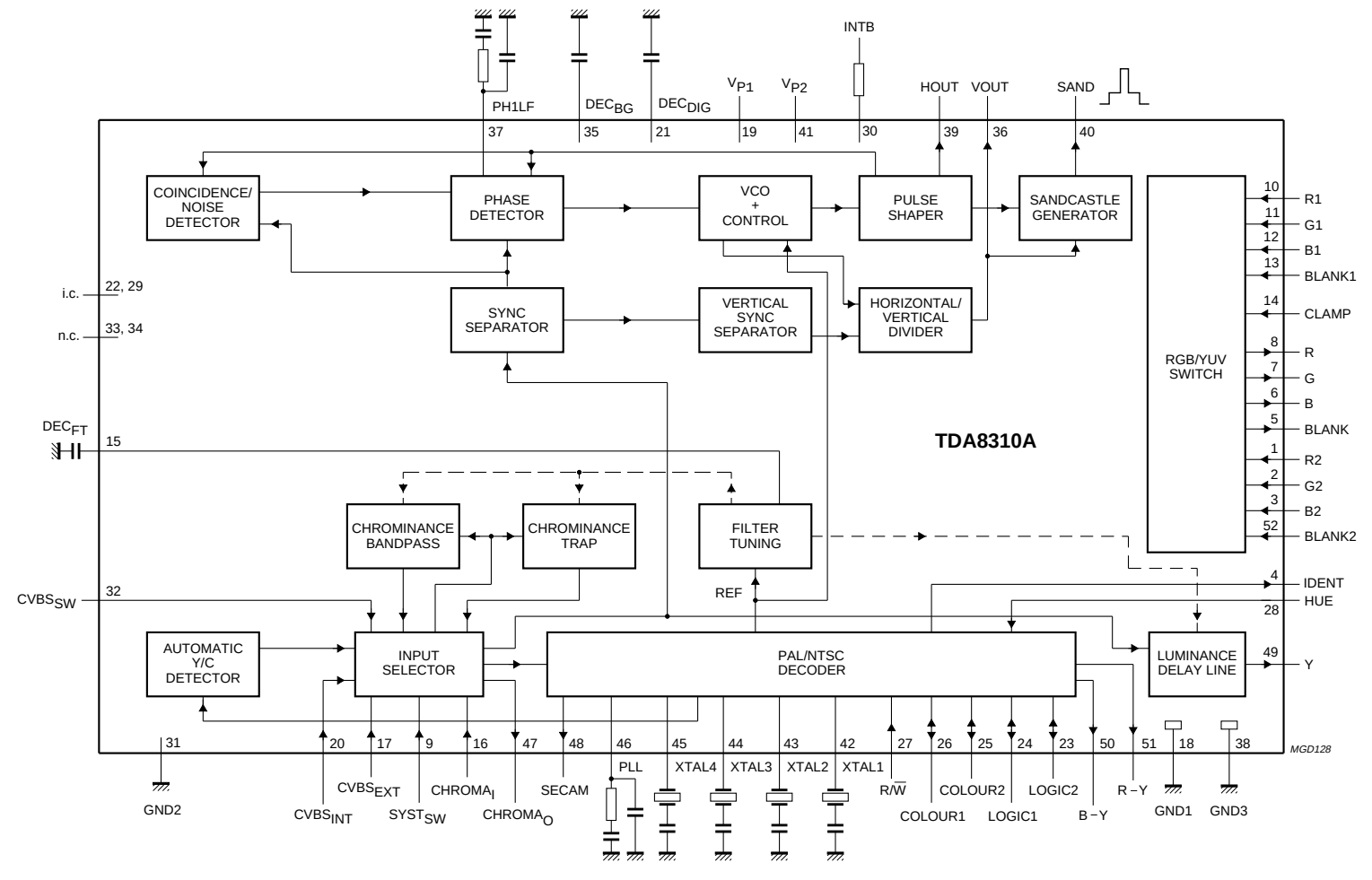
The circuit contains a chrominance bandpass and trap circuit. The filters are realised by gyrator circuits that are automatically tuned by comparing the tuning frequency with the crystal frequency of the decoder. When a Y/C signal is supplied to the input the chrominance trap is automatically switched off by the Y/C detection circuit however, it is also possible to force the filters in the CVBS or Y/C position.
The luminance delay line is also realised by gyrator circuits.

Colour decoder

The colour decoder contains an alignment-free crystal oscillator, a colour killer circuit and colour difference demodulators. The 90° phase shift for the reference signal is achieved internally.
The colour decoder is very flexible. Together with the SECAM decoder (TDA8395) an automatic multistandard decoder can be designed but it is also possible to use it for one standard when only one crystal is connected to the IC.
The decoder can be forced to one of the standards via the 'forced mode' pins. The crystal pins which are not used must be connected to the positive supply line via a 8.2 kΩ resistor. It is also possible to connect the non-used pins with one resistor to the positive supply line. In this event the resistor must have a value of 8.2 kΩ divided by the number of pins.
The chrominance output signal of the video switch is externally available and must be used as an input signal for the SECAM decoder.

RGB/YUV switch

The RGB/YUV switch is for switching between two RGB or YUV video sources. The outputs of the switch can be set to high-impedance state so that other switches can be used in parallel.
The switch is controlled via pins 13 and 52.


PH1LF
DEC_BG
DEC_DIG
V_P1
V_P2
INTB
HOUT
VOUT
SAND
37
35
21
19
41
30
39
36
40
COINCIDENCE/ NOISE DETECTOR
PHASE DETECTOR
VCO + CONTROL
PULSE SHAPER
SANDCASTLE GENERATOR
SYNC SEPARATOR
VERTICAL SYNC SEPARATOR
HORIZONTAL/ VERTICAL DIVIDER
RGB/YUV SWITCH
TDA8310A
i.c.
22, 29
n.c.
33, 34
DEC_FT
15
CHROMINANCE BANDPASS
CHROMINANCE TRAP
FILTER TUNING
REF
CVBS_SW
32
AUTOMATIC Y/C DETECTOR
INPUT SELECTOR
PAL/NTSC DECODER
LUMINANCE DELAY LINE
10
R1
11
G1
12
B1
13
BLANK1
14
CLAMP
8
R
7
G
6
B
5
BLANK
1
R2
2
G2
3
B2
52
BLANK2
4
IDENT
28
HUE
49
Y
31
GND2
20
CVBS_INT
17
CVBS_EXT
9
SYST_SW
16
CHROMA_I
47
CHROMA_O
48
SECAM
46
PLL
45
XTAL4
44
XTAL3
43
XTAL2
42
XTAL1
27
R/W
26
COLOUR1
25
COLOUR2
24
LOGIC1
23
LOGIC2
50
B−Y
51
R−Y
18
GND1
38
GND3
MGD128

PINNING

SYMBOL	PIN	DESCRIPTION
R2	1	RED input 2 (PIP)
G2	2	GREEN input 2 (PIP)
B2	3	BLUE input 2 (PIP)
IDENT	4	colour standard identification output
BLANK	5	blanking output
B	6	BLUE output
G	7	GREEN output
R	8	RED output
$SYST_{SW}$	9	CVBS/system switch
R1	10	RED input 1
G1	11	GREEN input 1
B1	12	BLUE input 1
BLANK1	13	blanking input 1
CLAMP	14	clamping pulse input
DEC_{FT}	15	decoupling filter tuning
$CHROMA_I$	16	chrominance input
$CVBS_{EXT}$	17	external CVBS/Y input
GND1	18	ground 1 (0 V)
V_{P1}	19	supply voltage 1 (+8 V)
$CVBS_{INT}$	20	internal CVBS input
DEC_{DIG}	21	decoupling digital supply rail
i.c.	22	internally connected (test purposes)
LOGIC2	23	crystal logic 2 input/output
LOGIC1	24	crystal logic 1 input/output
COLOUR2	25	colour system logic 2 input/output
COLOUR1	26	colour system logic 1 input/output
$R/\overline{W}$	27	read/write selection input

SYMBOL	PIN	DESCRIPTION
HUE	28	HUE control input
i.c.	29	internally connected (test purposes)
INTB	30	internal bias
GND2	31	ground 2 (0 V)
$CVBS_{SW}$	32	CVBS positive/negative modulation control switch input
n.c.	33	not connected
n.c.	34	not connected
DEC_{BG}	35	bandgap decoupling
VOUT	36	vertical sync output pulse
PH1LF	37	phase 1 loop filter
GND3	38	ground 3 (0 V)
HOUT	39	horizontal sync output pulse
SAND	40	sandcastle pulse output
V_{P2}	41	supply voltage 2 (+8 V)
XTAL1	42	4.4336 MHz crystal
XTAL2	43	3.5820 MHz crystal for PAL-N
XTAL3	44	3.5756 MHz crystal for PAL-M
XTAL4	45	3.5795 MHz crystal for NTSC
PLL	46	PLL colour filter
$CHROMA_O$	47	chrominance output for TDA8395
SECAM	48	SECAM reference output
Y	49	Y output
B–Y	50	B–Y output
R–Y	51	R–Y output
BLANK2	52	blanking/insertion input 2 (PIP)

TDA8395

SECAM DECODER

FEATURES

- Fully integrated filters
- Alignment free
- For use with baseband delay

GENERAL DESCRIPTION

The TDA8395 is a self-calibrating, fully integrated SECAM decoder. The IC should preferably be used in conjunction with the PAL/NTSC decoder TDA8362 or TDA8366 and with the switched capacitor baseband delay circuit TDA4660. The IC incorporates HF and LF filters, a demodulator and an identification circuit (luminance is not processed in this IC). The IC needs no adjustments and very few external components are required. A highly stable reference frequency is required for calibration and a two-level sandcastle pulse for blanking and burst gating.

FUNCTIONAL DESCRIPTION

The TDA8395 is a self-calibrating SECAM decoder designed for use with a baseband delay circuit.

During frame retrace a 4.433619 MHz reference frequencyis used to calibrate the filters and the demodulator. Thereference frequency should be very stable during this period.

The Cloche filter is a gyrator-capacitor type filter theresonance frequency of which is controlled during the calibration period and offset during scan; this ensures thecorrect frequency during calibration.

The demodulator is a Phase-Locked Loop (PLL) type demodulator which uses the frequency reference and the bandgap reference to force the PLL to the required demodulation characteristic.

The low frequency de-emphasis is matched to the PLL and is controlled by the tuning voltage of the PLL.

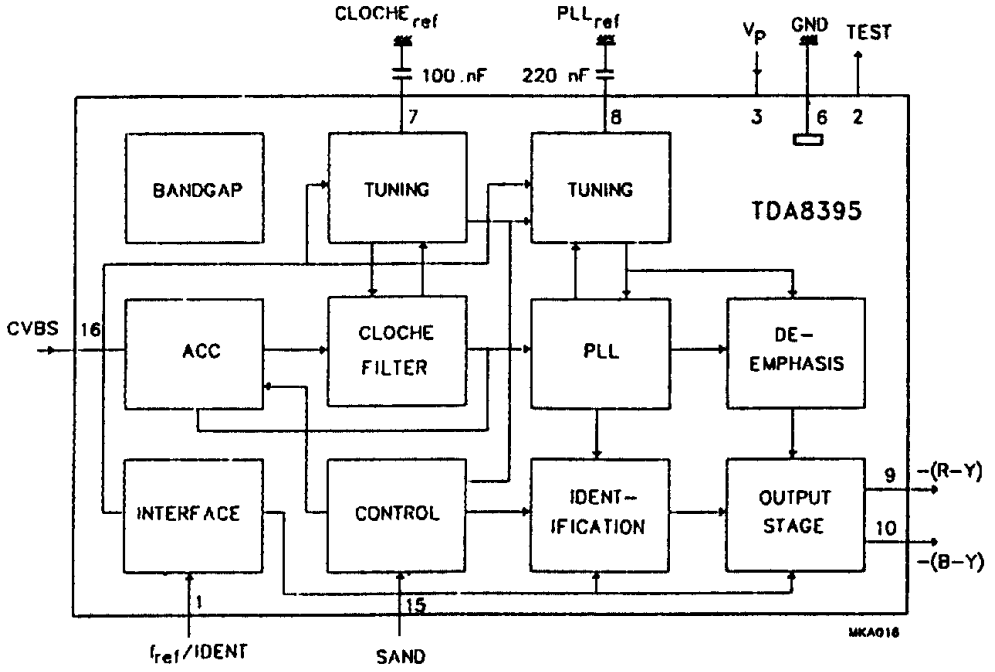


Fig.1 Block diagram.

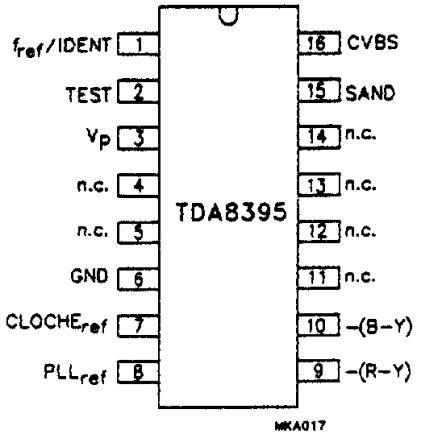


Fig.2 Pin configuration

PINNING

SYMBOL	PIN	DESCRIPTION
f_{ref}/ IDENT	1	reference frequency input/identification input
TEST	2	test output
V_P	3	positive supply voltage
n.c.	4	not connected
n.c.	5	not connected
GND	6	ground
$CLOCHE_{ref}$	7	Cloche reference filter
PLL_{ref}	8	PLL reference
–(R–Y)	9	–(R–Y) output
–(B–Y)	10	–(B–Y) output
n.c.	11	not connected
n.c.	12	not connected
n.c.	13	not connected
n.c.	14	not connected
SAND	15	sandcastle pulse input
CVBS	16	video (chrominance) input

A digital identification circuit scans the incoming signal for SECAM (only line-identification is implemented). The identification circuit needs to communicate with theTDA8362 to guarantee that the output signal from the decoder is only available when no PAL signal has been identified. If a SECAM signal is decoded a request for colour-on is transmitted to pin 1 (current is sunk). If the signal request is granted (i.e. pin 1 is HIGH therefore no PAL) the colour difference outputs (-(B-Y) and -(P-Y)) from the TDA8362 are high impedance and the output signals from the TDA8395 are switched ON. If no SECAM signal is decoded during a two-frame period the demodulator will be initialized before another attempt is made also during a two-frame period. The CD outputs will be blanked or high-impedance depending on the logic level at pin 1.

A two-level sandcastle pulse generates the required blanking periods and, also, clocks the digital identification pulse on the falling edge of the burst gate pulse. To enable The calibration period to be defined the vertical retrace is discriminated from the horizontal retrace, this is achieved by measuring the width of the blanking period.

TEA6415C

BUS-CONTROLLED VIDEO MATRIX SWITCH

DESCRIPTION

- 20MHz BANDWIDTH
- CASCADABLE WITH ANOTHER TEA6415C (INTERNAL ADDRESS CAN BE CHANGED BY PIN 7VOLTAGE)
- INPUTS (CVBS, RGB, MAC, CHROMA, ...)
- POSSIBILITY OF MAC OR CHROMA SIGNAL
- FOR EACH INPUT BY SWITCHING-OFF THE
- CLAMP WITH AN EXTERNAL RESISTOR BRIDGE
- BUS CONTROLLED
- 6.5dB GAIN BETWEEN ANY INPUT AND OUT-PUT
- -55dB CROSSTALK AT 5MHz
- FULLY ESD PROTECTED

GENERALDESCRIPTION

The mainfunctionof the IC is to switch 8 video input sources on 6 outputs.
Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals).
Each nominal gain between any input and output is 6.5dB. For D2MAC or Chroma signal the align-ment is switched off by forcing, with an external resistor bridge, 5 VDC on the input. Each input can be used as a normal input or as a MAC or Chroma input (with external resistor bridge). All the switch-ing possibilities are changed through the BUS.
Driving 75Ω load needs an external transistor. It is possible to have the same input connected to several outputs.
The starting configuration upon power on (power supply : 0 to 10V) is undetermined. In this case, 6 words of 16 bits are necessary to determine one configuration. In other case, 1 word of 16 bits is necessary to determine one configura-tion

TDA4665

Baseband delay line

FEATURES

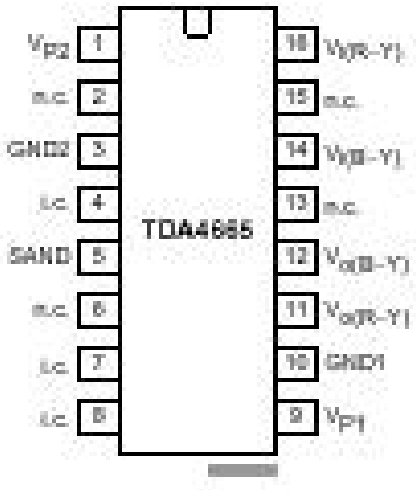
- Two comb filters, using the switched-capacitor technique, for one line delay time (64 ms)
- Adjustment-free application
- No crosstalk between SECAM colour carriers (diaphoty)
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals (±(P-Y) and ±(B-Y))
- VCO without external components
- 3 MHz internal clock signal derived from a 6 MHz CCO, line-locked by the sandcastle pulse (64 ms line)
- Sample-and-hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Addition of delayed and non-delayed output signals
- Output buffer amplifiers
- Comb filtering functions for NTSC colour-difference signals to suppress cross-colour

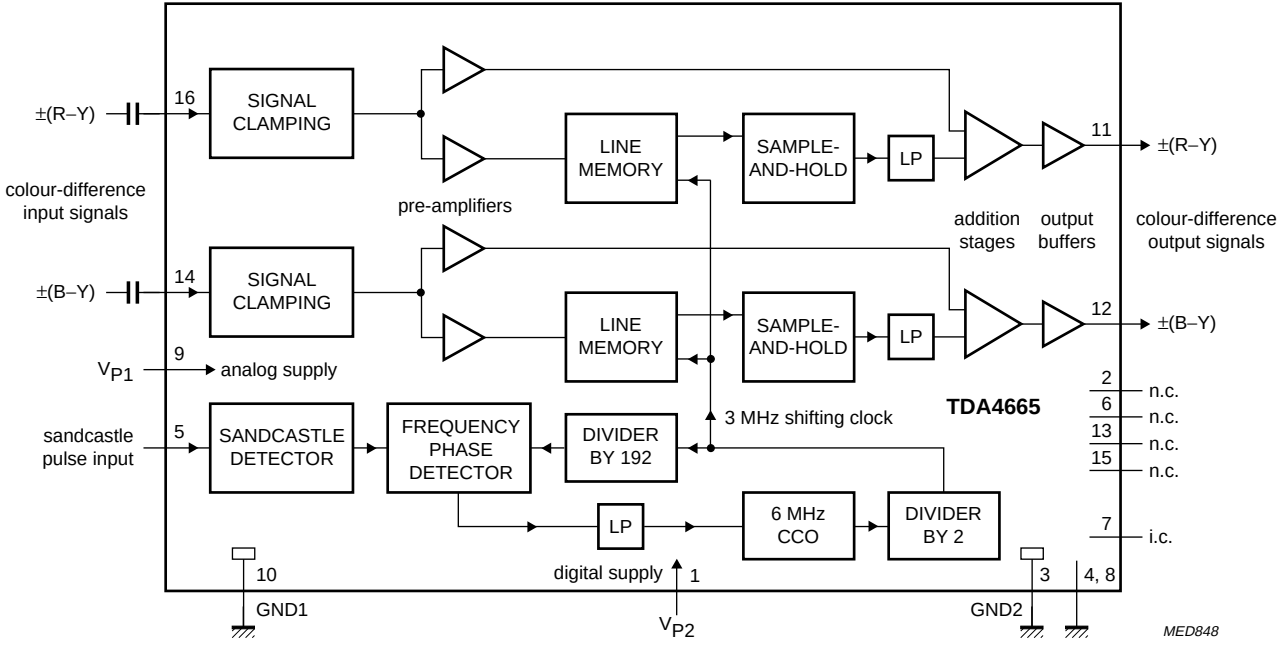
GENERAL DESCRIPTION

The TDA4665 is an integrated baseband delay line circuit with one line delay. It is suitable for decoders with colour-difference signal outputs ±(P-Y) and ±(B-Y).

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P2}	1	+5 V supply voltage for digital part
n.c.	2	not connected
GND2	3	ground for digital part (0 V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
i.c.	7	internally connected
i.c.	8	internally connected
V_{P1}	9	+5 V supply voltage for analog part
GND1	10	ground for analog part (0 V)
$V_{o(R-Y)}$	11	±(R–Y) output signal
$V_{o(B-Y)}$	12	±(B–Y) output signal
n.c.	13	not connected
$V_{i(B-Y)}$	14	±(B–Y) input signal
n.c.	15	not connected
$V_{i(R-Y)}$	16	±(R–Y) input signal




±(R–Y)
16
SIGNAL CLAMPING
LINE MEMORY
SAMPLE-AND-HOLD
LP
11
±(R–Y)
colour-difference input signals
pre-amplifiers
addition stages
output buffers
colour-difference output signals
±(B–Y)
14
SIGNAL CLAMPING
LINE MEMORY
SAMPLE-AND-HOLD
LP
12
±(B–Y)
V_{P1}
9
analog supply
TDA4665
2
n.c.
6
n.c.
13
n.c.
15
n.c.
3 MHz shifting clock
sandcastle pulse input
5
SANDCASTLE DETECTOR
FREQUENCY PHASE DETECTOR
DIVIDER BY 192
LP
6 MHz CCO
DIVIDER BY 2
7
i.c.
10
GND1
digital supply
1
V_{P2}
3
GND2
4, 8
MED848

SAA55xx

Standard TV microcontrollers with On-Screen Display (OSD)

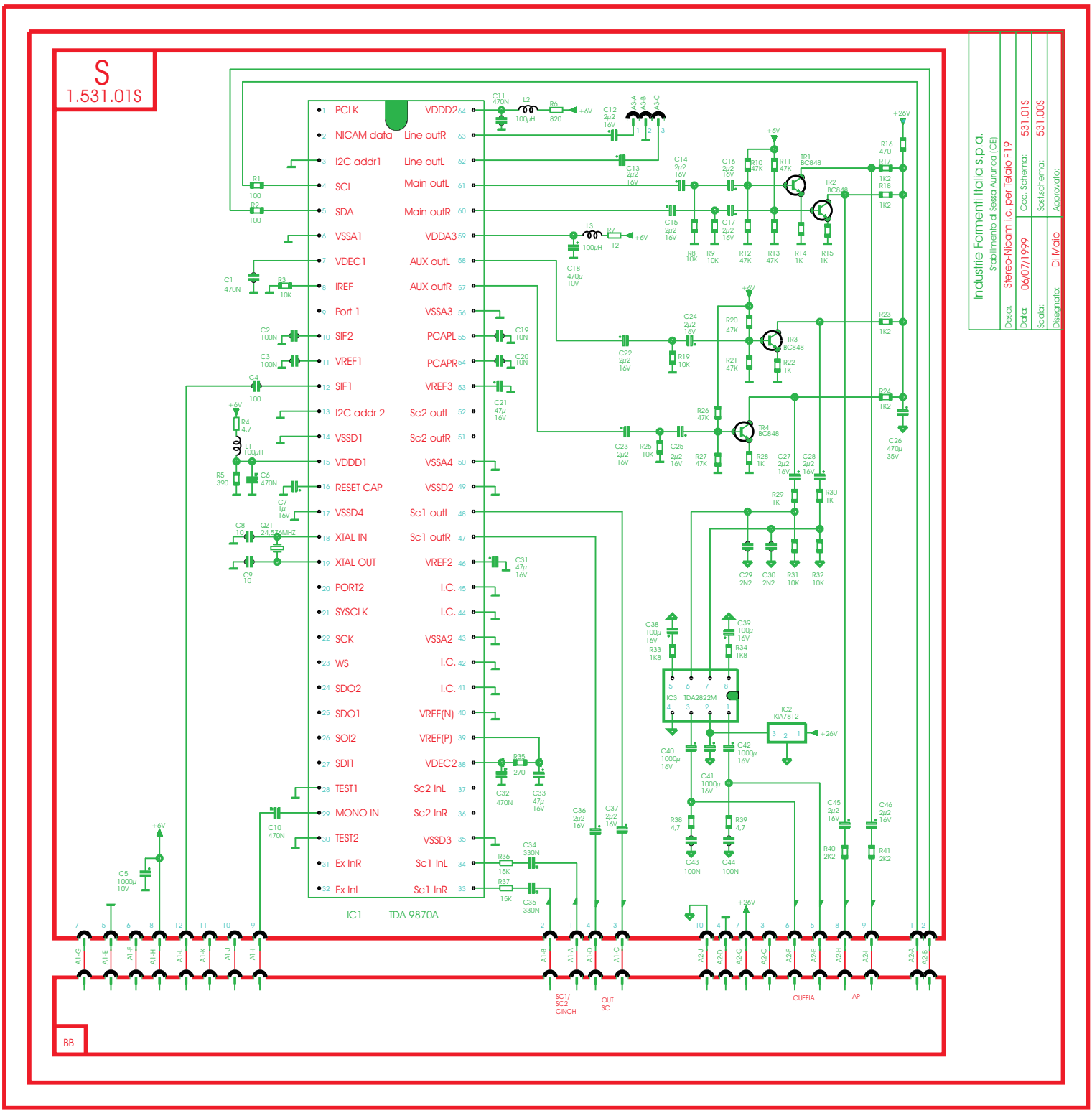
1 FEATURES

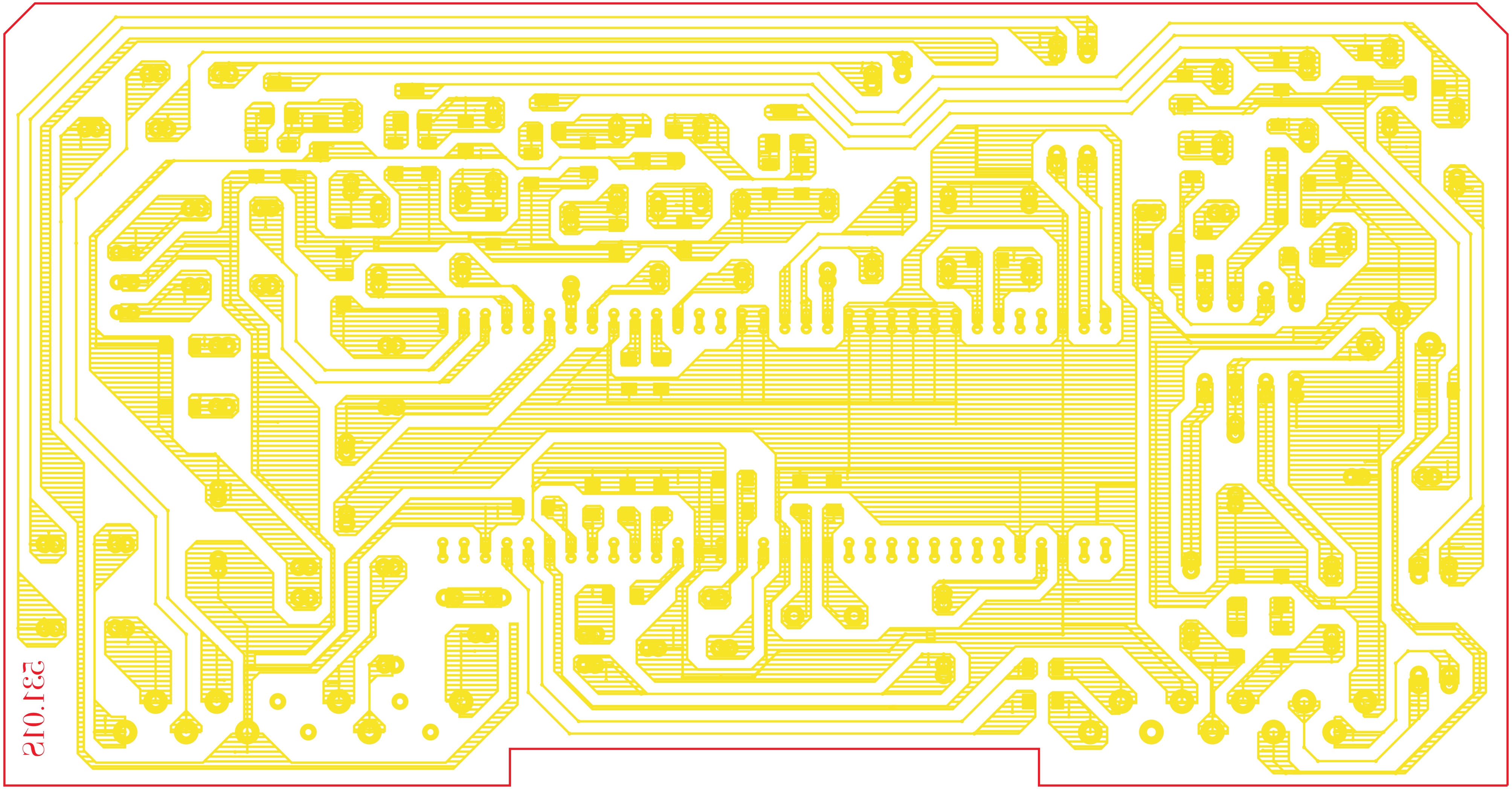
- Single-chip microcontroller with integrated On-Screen Display (OSD)
- Versions available with integrated data capture
- One Time Programmable (OTP) memory for both program Read Only Memory (ROM) and character sets
- Single power supply: 3.0 to 3.6 V
- 5 V tolerant digital inputs and I/O
- 29 I/O lines via individual addressable controls
- Programmable I/O for push-pull, open-drain and quasi-bidirectional
- Two port lines with 8 mA sink (at <0.4 V) capability, for direct drive of Light Emitting Diode (LED)
- Single crystal oscillator for microcontroller, OSD and data capture
- Power reduction modes: Idle and Power-down
- Byte level I 2 C-bus with dual port I/O
- Pin compatibility throughout family
- Operating temperature: -20 to +70 °C.

2 GENERAL DESCRIPTION

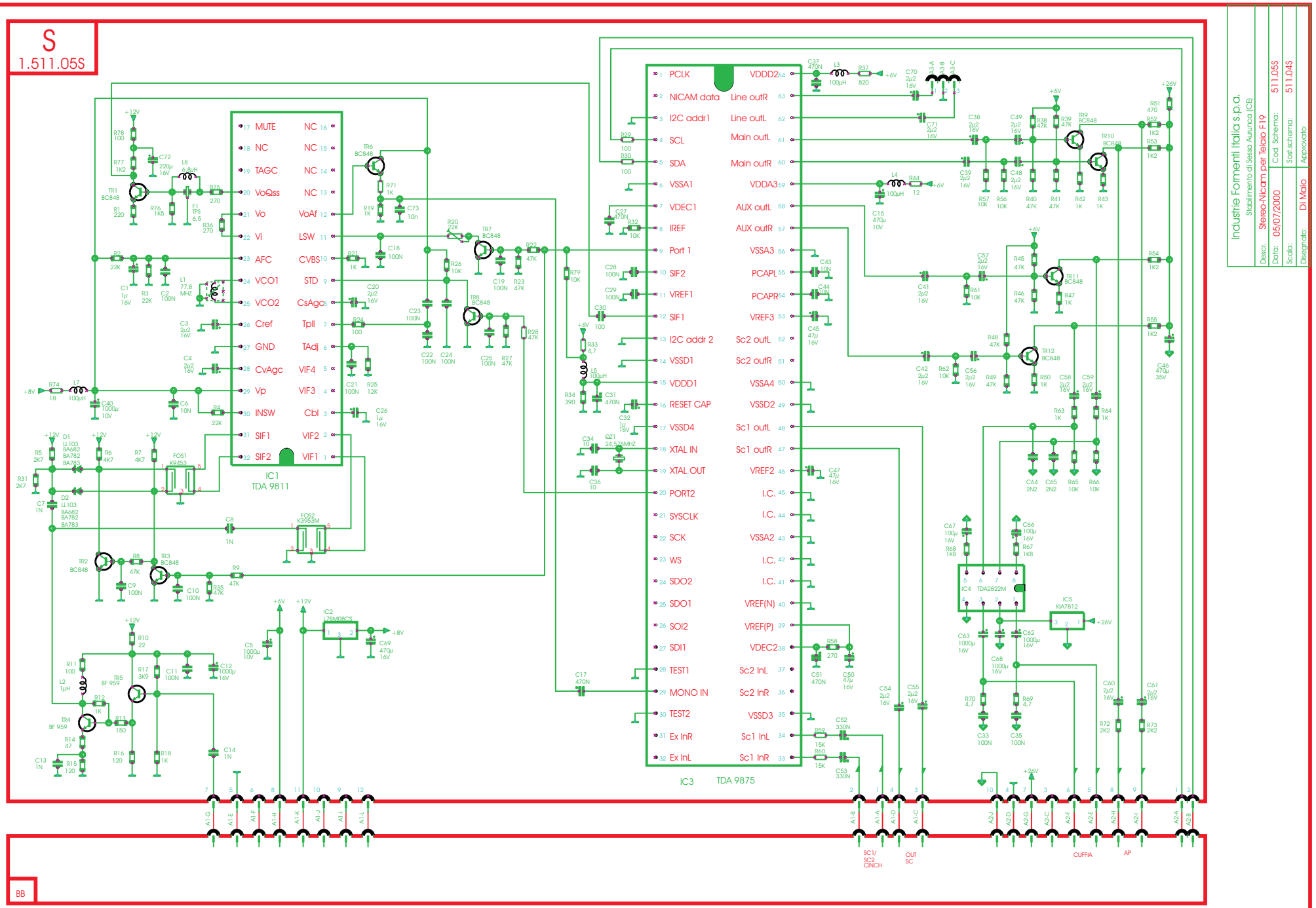
The SAA55xx standard family of microcontrollers are a derivative of the Philips industry-standard 80C51 microcontroller, and are intended for use as the central control mechanism in a television receiver. They provide control functions for the television system, OSD, and some versions include an integrated data capture and display function. The data capture hardware has the capability of decoding and displaying both 525 and 625-line World System Teletext (WST), Video Programming System (VPS) and Wide Screen Signalling (WSS) information. The same display hardware is used both for Teletext and OSD, which means that the display features available give greater flexibility to differentiate the TV set.

The SAA55xx standard family offers a range of functionality from non-text, 16-kbyte program ROM and 256-byte Random Access Memory (RAM), to a 10-page text version, 64-kbyte program ROM and 1.2-kbyte RAM.


S
1.531.01S
Industrie Formenti Italia s.p.a.
Stabilimento di Sessa Aurunca (CE)
Descr: Stereo-Nicam I.c. per Telaio F19
Data: 06/07/1999
Scala:
Cod. Schema: 531.01S
Sost.schema: 531.00S
Approvato:
Disegnato: Di Maio
IC1 TDA 9870A
PCLK
NICAM data
I2C addr1
SCL
SDA
VSSA1
VDEC1
IREF
Port 1
SIF2
VREF1
SIF1
I2C addr 2
VSSD1
VDDD1
RESET CAP
VSSD4
XTAL IN
XTAL OUT
PORT2
SYSCLK
SCK
WS
SDO2
SDO1
SOI2
SDI1
TEST1
MONO IN
TEST2
Ex InR
Ex InL
VDDD2
Line outR
Line outL
Main outL
Main outR
VDDA3
AUX outL
AUX outR
VSSA3
PCAPL
PCAPR
VREF3
Sc2 outL
Sc2 outR
VSSA4
VSSD2
Sc1 outL
Sc1 outR
VREF2
I.C.
VSSA2
VREF(N)
VREF(P)
VDEC2
Sc2 InL
Sc2 InR
VSSD3
Sc1 InL
Sc1 InR
IC2 KIA7812
IC3 TDA2822M
TR1 BC848
TR2 BC848
TR3 BC848
TR4 BC848
SC1/ SC2 CINCH
OUT SC
CUFFIA
AP
BB

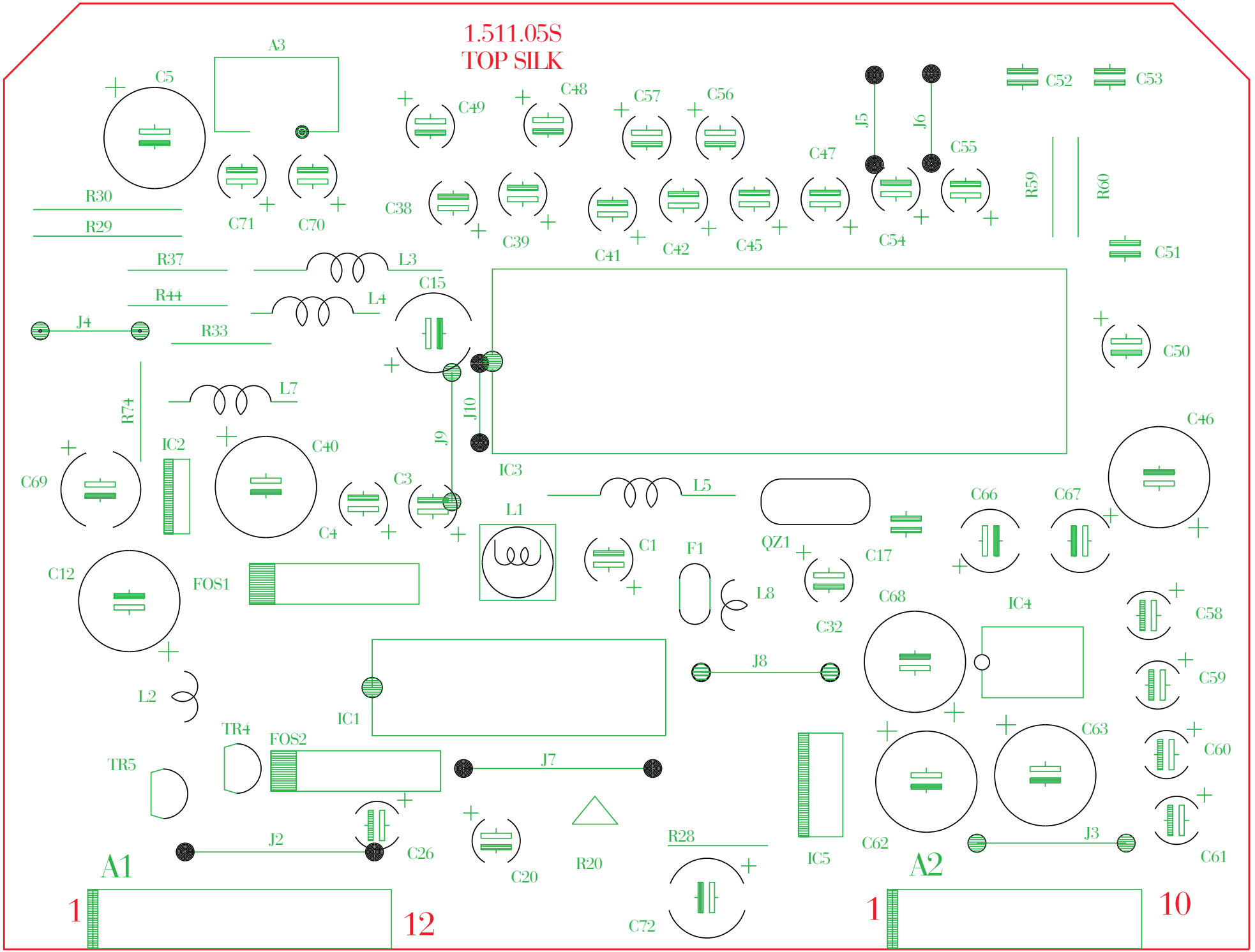


S
1.511.05S



Industrie Formenti Italia s.p.a.	
Stabilimento di Sesso Aurunca (CE)	
Descr:	Stereo-Nicam per telaio F19
Data:	05/07/2000
Scala:	
Disegnato:	Di Maio
Cod. Schema:	511.05S
Sost.schema:	511.04S
Approvato:	

BB


1.511.05S
TOP SILK
A3
C5
C49
C48
C57
C56
C52
C53
J5
J6
C55
C47
C54
R59
R60
C51
C38
C39
C41
C42
C45
R30
R29
C71
C70
R37
L3
R44
L4
C15
J4
R33
C50
L7
R74
J10
J9
IC2
C40
C46
C69
IC3
C3
C4
L5
C66
C67
L1
C1
F1
QZ1
C17
C12
FOS1
L8
C68
IC4
C58
C32
J8
C59
L2
IC1
C63
TR4
FOS2
C60
TR5
J7
C26
J2
C20
R20
R28
IC5
C62
J3
C61
A1
A2
C72
1
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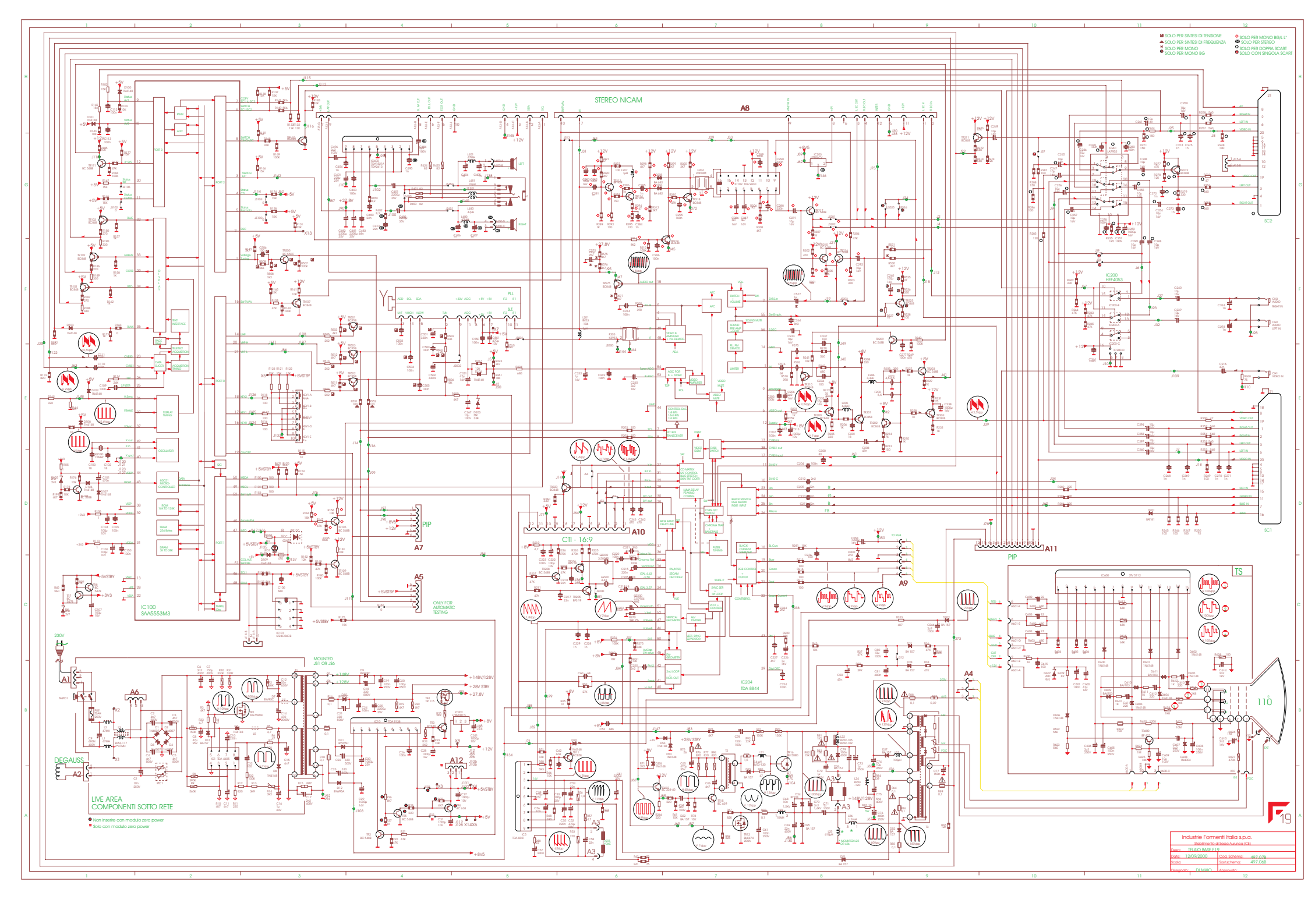
1
10

BOLTEC
1.911.052


SOLO PER SINTESI DI TENSIONE
SOLO PER SINTESI DI FREQUENZA
SOLO PER MONO
SOLO PER MONO BG
SOLO PER MONO BG/L L'
SOLO PER STEREO
SOLO PER DOPPIA SCART
SOLO CON SINGOLA SCART
STEREO NICAM
A8
IC100
SAA5553M3
PIP
A7
A5
ONLY FOR AUTOMATIC TESTINS
CTI - 16:9
A10
A11
A9
A4
IC204
TDA 8844
IC200
HEF4053
SC2
SC1
TS
230V
A1
A6
A2
DEGAUSS
MOUNTED JS1 OR JS6
A12
A3
LIVE AREA
COMPONENTI SOTTO RETE
Non inserire con modulo zero power
Solo con modulo zero power
Industrie Formenti Italia s.p.a.
Stabilimento di Sesto Aurunca (CE)
Disegno: TELAIO BASE F19
Data: 12/09/2000
Cod. Schema: 497.078
Scala:
Sost.schema: 497.068
Disegnato: DI MAIO
Aggiornato:
F19

TUNER
A8
A13
A10
A11
A9
A7
A4
A5
A6
A12
A400
MICROCONTROLLER
HEF4053
LA7955
497.06B
497.07B
F19
T2AH
230Vac
LIVE AREA
00 01 02 03 04 05
GEMAMIGLASOND

497.07B